

	No. 2156B	LC6554D,6554H
	4K-Byte ROM-Contained Single-Chip 4-Bit Microcomputers with FLT, LED Drivers	

The LC6554D/H are single-chip 4-bit microcomputers that contain a 4K-byte ROM, 1K-bit RAM, and have 64 pins. The LC6554D/H have 57 pins for ports — 28 pins for 7 input/output common ports, 21 pins for 6 output ports, and 8 pins for 2 input ports. The LC6554D/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function and burst pulse output function. Each of the 28 pins for input/output common ports contains a driver with a withstand voltage of 15V max. and a drive current of 15mA max. and each of the 21 pins for output ports contains a high-voltage output driver of the P-channel open drain type. Since the high-voltage output driver can be used as general-purpose high-current driver as well as fluorescent tube driver, the LC6554D/H can be also widely used in applications where no fluorescent display is provided.

The LC6554D/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and also made easier-to-use in the standby function.

Features

- Instruction set with 80 instructions (Common to the LC6500 series)
- On-chip 4096-byte ROM, 1024-bit RAM
- Instruction cycle time: 2.85 μ s (D version, $V_{DD} = 4$ to 5.5V)
0.92 μ s (H version, $V_{DD} = 4.5$ to 5.5V)
- Serial input/output interface x 1 (4 bit/8 bit program-selectable)
- I/O ports: 57 pins in all

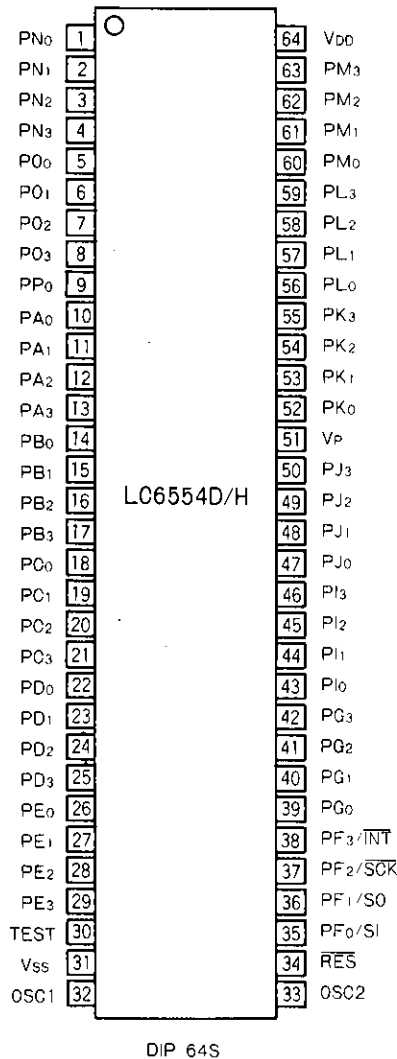
Input ports	8 pins
Input/output common ports	28 pins: 15V max., 15 mA max., LED drivable, pull-up resistance option available
Output ports	21 pins: V_{DD} —45 V withstand voltage, FLT drivable, common with general-purpose output, pull-down resistance option available
- Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.
- Interrupt function

Timer interrupt:	1
$\overline{INT}$ pin or serial I/O interrupt:	1
- Stack level: 8 levels (Common with interrupt)
- Timer: 4-bit prescaler + 8-bit programmable timer
- Burst pulse (64 x cycle time output function)
- Oscillator option

Circuit mode:	Ceramic resonator mode, RC mode, external clock mode (384 kHz to 4.33 MHz)
Predivider option:	1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction. Provides the function to absorb the OSC stabilizing time in the ceramic resonator mode.
- Supply Voltage: 4 to 5.5 V (D version)
4.5 to 5.5 V (H version)
- Package: DIP64 shrink type, QIP64

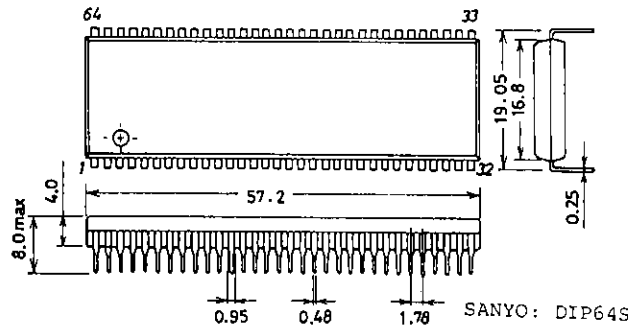
LC6554D, 6554H

Pin Assignment

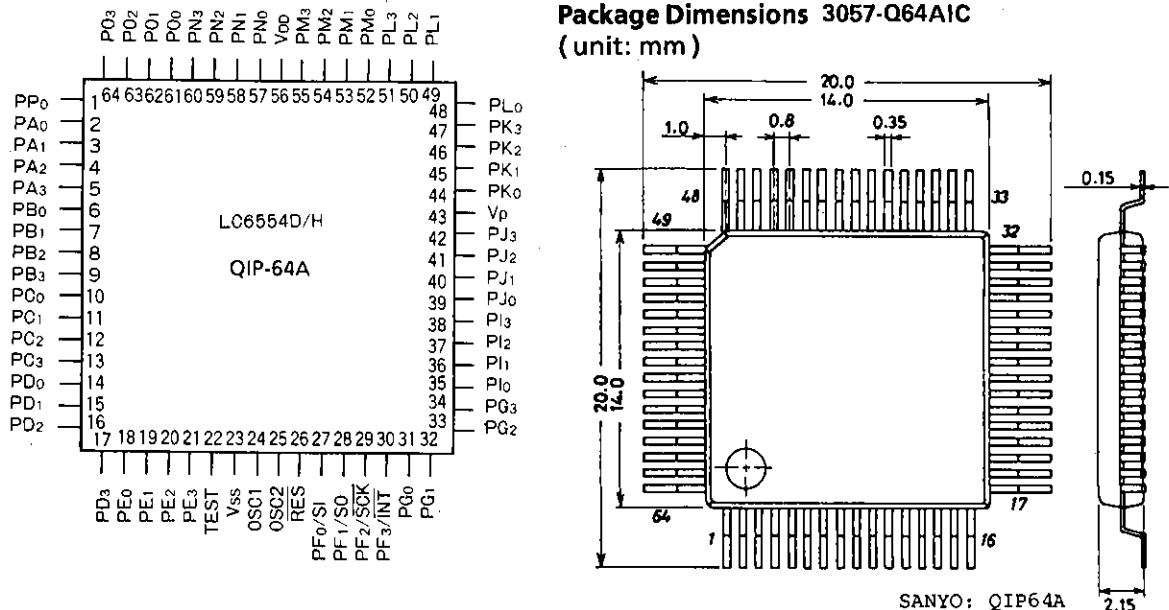


- OSC1, OSC2 : C, R, or ceramic resonator oscillator for OSC
- PA₀₋₃ : Port for input only A₀₋₃
- PB₀₋₃ : Port for input only B₀₋₃
- PC₀₋₃ : Input/output common port C₀₋₃
- PD₀₋₃ : Input/output common port D₀₋₃
- PE₀₋₃ : Input/output common port E₀₋₃
- PF₀₋₃ : Input/output common port F₀₋₃
- PG₀₋₃ : Input/output common port G₀₋₃
- PI₀₋₃ : Input/output common port I₀₋₃
- PJ₀₋₃ : Input/output common port J₀₋₃
- PK₀₋₃ : Port for output only K₀₋₃
- PL₀₋₃ : Port for output only L₀₋₃
- PM₀₋₃ : Port for output only M₀₋₃
- PN₀₋₃ : Port for output only N₀₋₃
- PO₀₋₃ : Port for output only O₀₋₃
- PP₀ : Port for output only P₀
- SI : 4-bit/8-bit serial input port
- SO : 4-bit/8-bit serial output port
- SCK : Input/output for serial clock
- INT : Interrupt request input
- V_P : V_P pin
- RES : Reset
- TEST : Test
- With high-voltage output driver

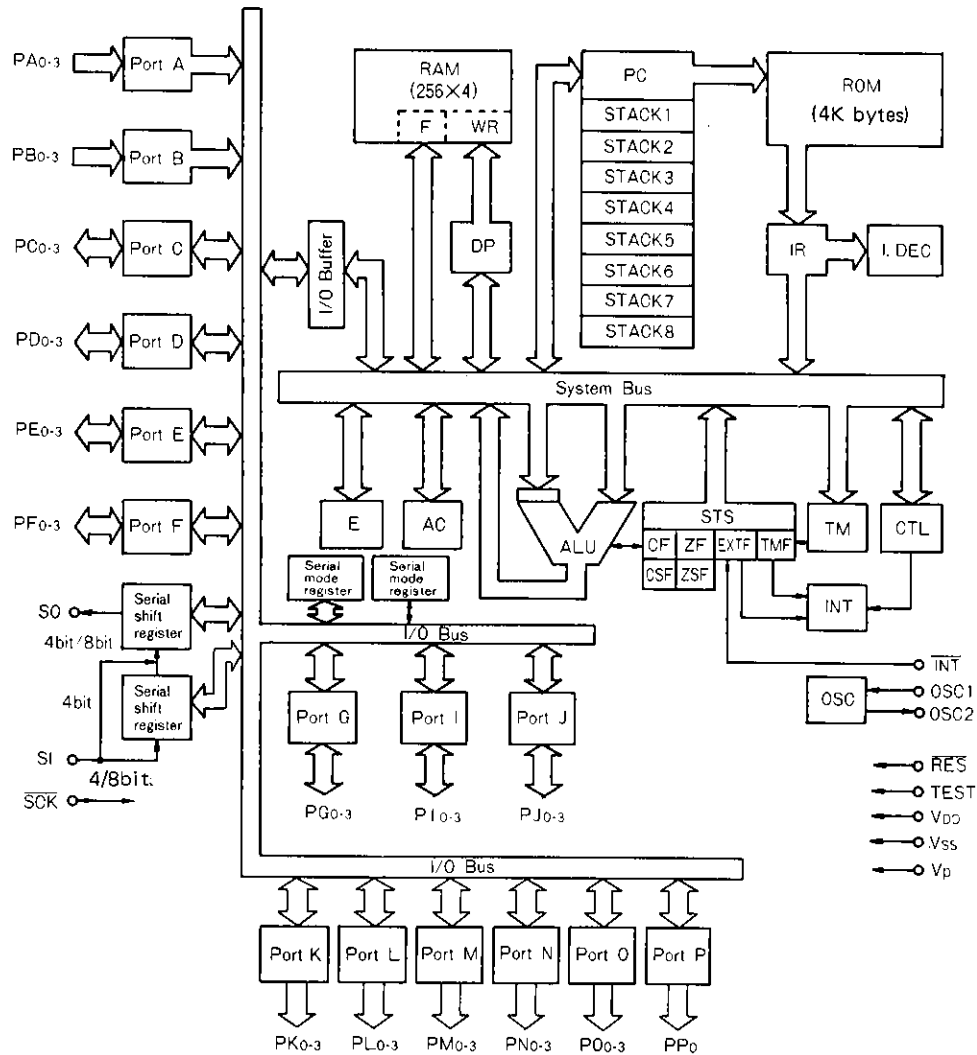
Package Dimensions 3071-D64IC (unit: mm)



Package Dimensions 3057-Q64AIC (unit: mm)



System Block Diagram



RAM	: Data memory	STS	: Status register
F	: Flag	ROM	: Program memory
WR	: Working register	PC	: Program counter
AC	: Accumulator	INT	: Interrupt control
ALU	: Arithmetic and logic unit	IR	: Instruction register
DP	: Data pointer	I.DEC	: Instruction decoder
E	: E register	CF, CSF	: Carry flag, carry save flag
CTL	: Control register	ZF, ZSF	: Zero flag, zero save flag
OSC	: Oscillator	EXTF	: External interrupt request
TM	: Timer	TMF	: Internal interrupt request

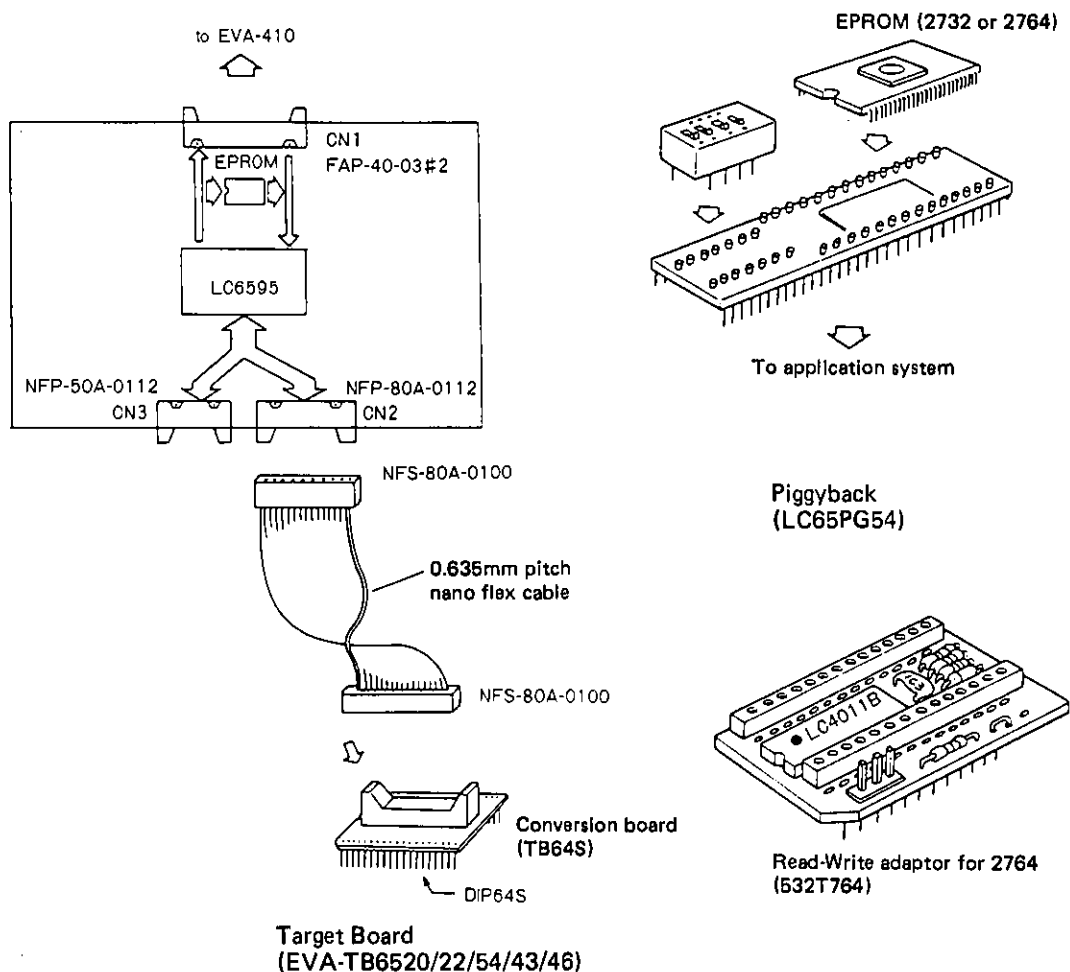
(Note) SI, SO, $\overline{SCK}$, $\overline{INT}$: Common to PF₀ to PF₃

Development Support Tools

The following are available to support the program development for the LC6554.

- (1) User's Manual
"LC6554 Series User's Manual" No. E21B (Issued in December, 1987)
- (2) Development Tool Manual
For the EVA-410 system, refer to the description of Development support tool in "LC6554 Series User's Manual".
For the EVA-800 system, refer to "EVA-800 · LC6554 Series Development Tool Manual".
- (3) Development Tools
 - 1) For program development (EVA-410 system)
 - i. (SDS-410) system
 - ii. CP/M80 base cross assembler: (LC6554, COM)
 - iii. Evaluation kit (EVA-410C)
 - iv. Target board (EVA-TB6520/22/54/43/46), evaluation dhip (LC6595)
 - 2) For program evaluation
 - i. Piggyback (LC65PG54)

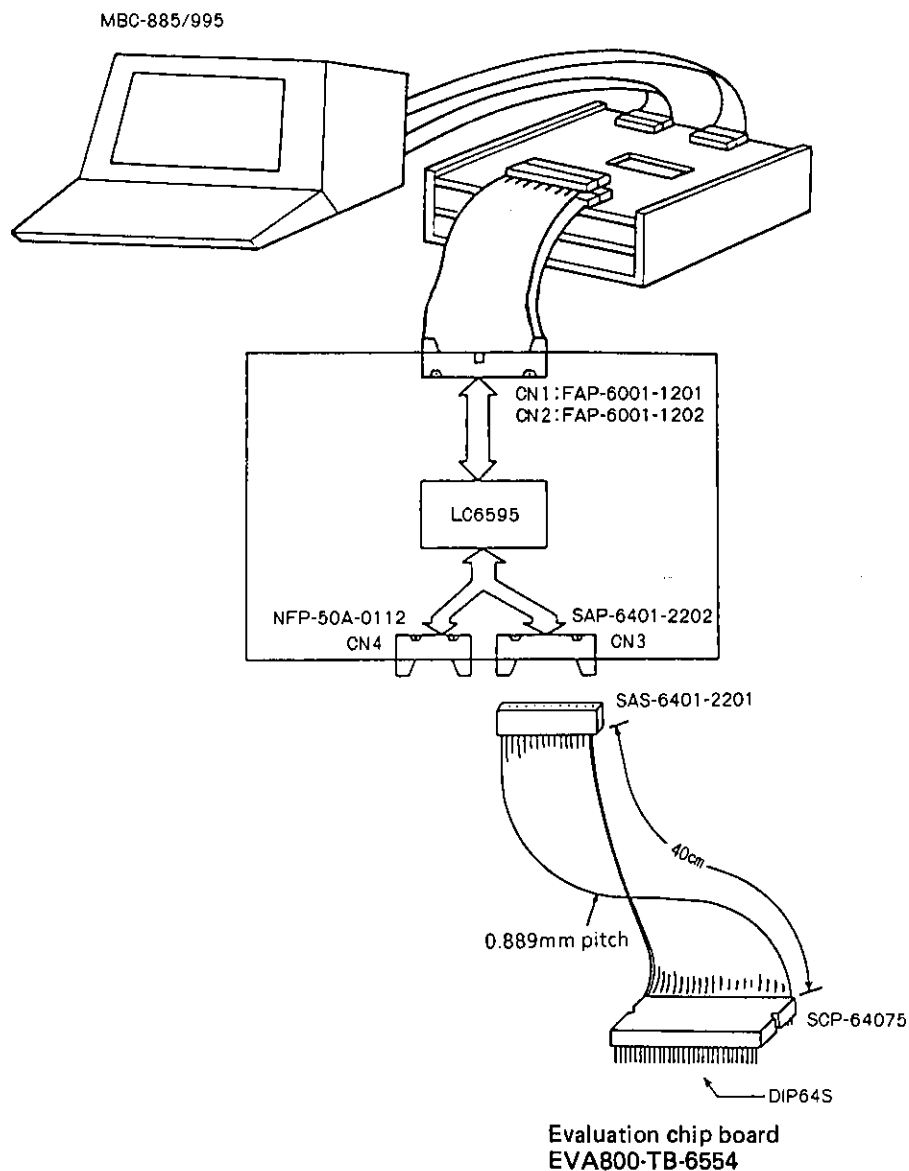
Note. For notes for program evaluation, do not fail to refer to "5-3-4. Notes when evaluating programs for the LC6554" in "LC6554 Series User's Manual".



(3) For program development (EVA-800 system)

- i. MBC-885/995 (IBM PC/XT, IBM PC-AT compatible) system and cross assembler
- ii. Cross assembler MS-DOS base cross assembler: (LC6554D.COM, LC6554H.COM)
- iii. Evaluation chip: LC6595
- iv. Emulator : EVA-800 control board and evaluation chip board

Appearance of Development Support System



(Note 1) IBM PC/XT, IBM PC-AT: Products of IBM Corporation

MS-DOS: Trademark of Microsoft Corporation

(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B, ...) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

Pin Description

Pin Name	Pins	I/O	Functions	Options	During Reset
VDD VSS	1 1	—	Power supply	—	—
OSC1	1	Input	- Pin for externally connecting R,C or a ceramic resonator for system clock generation - For the external clock mode, the OSC2 pin is open.	(1) External clock input (2) 2-pin RC OSC (3) 2-pin ceramic resonator OSC (4) Predivider option 1. No predivider 2. 1/3 predivider 3. 1/4 predivider	—
OSC2	1	Output			
PA0 PA1 PA2 PA3	4	Input	- Input port A0 to 3 (Low-threshold input) 4-bit input (IP instruction) - Single-bit decision (BP, BNP instructions)	—	—
PB0 PB1 PB2 PB3	4	Input	- Input port B0 to 3 (Low-threshold input) 4-bit input (IP instruction) - Single-bit decision (BP, BNP instructions) - Standby is controlled by the PB3. - The PB3 pin must be free from chattering during the HALT instruction execution cycle.	—	—
PC0 PC1 PC2 PC3	4	Input/output	- Input/output common port C0 to 3. 4-bit input (IP instruction) 4-bit output (OP instruction) - Single-bit decision (BP, BNP instructions) - Single-bit set/reset (SPB, RPB instructions) - Output ("H" or "L") during reset may be specified by option.	(1) Open drain type output (2) With pull-up resistance (3) Output during reset: "H" (4) Output during reset: "L" (1), (2): Specified bit by bit. (3), (4): Specified in a group of 4 bits.	"H" output "L" output (Option-selectable)
PD0 PD1 PD2 PD3	4	Input/output	Input/output common port D0 to 3. The functions, options are the same as for the PC0 to 3.	Same as for the PC0 to 3.	Same as for the PC0 to 3.
PE0 PE1 PE2 PE3	4	Input/output	- Input/output common port E0 to 3 4-bit input (IP instruction) 4-bit output (OP instruction) - Single-bit decision (BP, BNP instructions) - Single-bit set/reset (SPB, RPB instructions) - PE0: With burst pulse (64Tcyc) output function	(1) Open drain type output (2) With pull-up resistance (1), (2): Specified bit by bit.	"H" output (Output Nch transistor OFF)

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Pin Name	Pins	I/O	Functions	Options	During Reset
PF ₀ /SI PF ₁ /SO PF ₂ / $\overline{\text{SCK}}$ PF ₃ / $\overline{\text{INT}}$	4	Input/output	- Input/output port F₀ to 3 The functions, options are the same as for the PE₀ to 3. However, no burst pulse output function is provided. - PF₀ to 3: Also used for serial interface, $\overline{\text{INT}}$ input. Program-selectable. 4-bits/8 bits of serial input/output: Program-selectable SI: Serial input port SO: Serial output port $\overline{\text{SCK}}$: Serial clock input/output $\overline{\text{INT}}$: Interrupt request input	Same as for the PE ₀ to 3.	Same as for the PE ₀ to 3. Serial port: Disable Interrupt source: $\overline{\text{INT}}$
PG ₀ PG ₁ PG ₂ PG ₃	4	Input/output	Input/output common port G₀ to 3. The functions, options are the same as for the PE₀ to 3. However, no burst pulse output function is provided.	Same as for the PE ₀ to 3.	Same as for the PE ₀ to 3.
PI ₀ PI ₁ PI ₂ PI ₃	4	Input/output	Input/output common port I₀ to 3 The functions, options are the same as for the PG₀ to 3.	Same as for the PG ₀ to 3.	Same as for the PG ₀ to 3.
PJ ₀ PJ ₁ PJ ₂ PJ ₃	4	Input/output	Input/output common port J₀ to 3 The functions, options are the same as for the PG₀ to 3.	Same as for the PG ₀ to 3.	Same as for the PG ₀ to 3.
PK ₀ PK ₁ PK ₂ PK ₃	4	Output	Output port K₀ to 3 (Segment driver output) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions)	(1) Open drain type output (2) With pull-down resistance • (1), (2): Specified bit by bit.	"L" output (Output Pch transistor OFF)
PL ₀ PL ₁ PL ₂ PL ₃	4	Output	Output port L₀ to 3 (Segment driver output) The functions, options are the same as for the PK₀ to 3.	Same as for the PK ₀ to 3.	Same as for the PK ₀ to 3.
PM ₀ PM ₁ PM ₂ PM ₃	4	Output	Output port M₀ to 3 (Digit driver output) The functions, options are the same as for the PK₀ to 3.	Same as for the PK ₀ to 3.	Same as for the PK ₀ to 3.
PN ₀ PN ₁ PN ₂ PN ₃	4	Output	Output port N₀ to 3 (Digit driver output) The functions, options are the same as for the PK₀ to 3.	Same as for the PK ₀ to 3.	Same as for the PK ₀ to 3.

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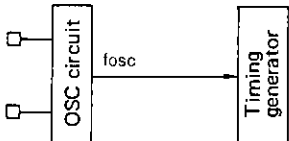
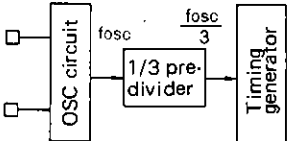
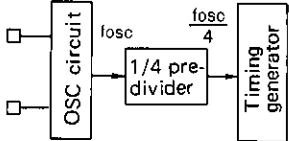
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Pin Name	Pins	I/O	Functions	Options	During Reset
PO ₀ PO ₁ PO ₂ PO ₃	4	Output	- Output port O₀ to 3 (Digit driver output) - The functions, options are the same as for the PK₀ to 3.	Same as for the PK ₀ to 3.	Same as for the PK ₀ to 3.
PP ₀	1	Output	- Output port P₀ (Digit driver output) - The functions, options are the same as for the PK₀ to 3. - This port consists of a single bit.	Same as for the PK ₀ to 3.	Same as for the PK ₀ to 3.
RES	1	Input	- System reset input - For power-up reset, C is connected externally. - For reset restart, "L" level is applied for 4 clock cycles or more.	—	—
TEST	1	Input	- LSI test pin - Normally connected to V_{SS}	—	—
V _p	1	—	Power supply pin for pull-down resistance	—	—

Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. External Clock		Input: Schmitt type.
2. 2-pin RC OSC		Input: Schmitt type.
3. Ceramic Resonator OSC		

Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider		• Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444 kHz. (LC6554D) • The OSC frequency, external clock do not exceed 4330 kHz. (LC6554H) • Refer to Table of OSC, Predivider Option (Table 2).
2. 1/3 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz. • Refer to Table of OSC, Predivider Option (Table 2).
3. 1/4 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz. • Refer to Table of OSC, Predivider Option (Table 2).

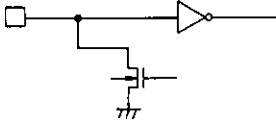
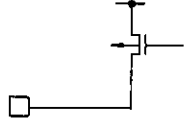
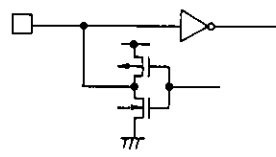
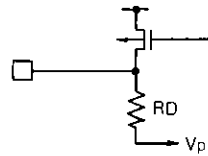
Options of Ports C, D Output Level during Reset

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports C, D
2. Output during reset: "L" level	All of 4 bits of ports C, D

Options of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (bitwise).

Option Name	Circuit	Applicable Ports
1. Open drain type output		Ports C, D, E, F, G, I, J
		Ports K, L, M, N, O, P
2. Output with pull-up resistance		Ports C, D, E, F, G, I, J
3. Output with pull-down resistance		Ports K, L, M, N, O, P

LC6554D

1. Absolute Maximum Ratings/ $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD\text{ max}}$	V_{DD}	-0.3 to +7.0	V
Output Voltage	$V_{O(1)}$	OSC2	Allowable up to voltage generated	V
	$V_{O(2)}$	Port K to P	$V_{DD}-45$ to $V_{DD}+0.3$	V
Input Voltage	$V_{I(1)}$	OSC1 (Note 1)	-0.3 to $V_{DD}+0.3$	V
	$V_{I(2)}$	TEST, $\overline{\text{RES}}$	-0.3 to $V_{DD}+0.3$	V
	$V_{I(3)}$	Port A, B	-0.3 to +15	V
	$V_{I(4)}$	V_p	$V_{DD}-45$ to $V_{DD}+0.3$	V
Input/Output Voltage	$V_{IO(1)}$	Port of OD type (Port C to J)	-0.3 to +15	V
	$V_{IO(2)}$	Port of PU type (Port C to J)	-0.3 to $V_{DD}+0.3$	V
Peak Output Current	$I_{OP(1)}$	Port C to J	-2 to +15	mA
	$I_{OP(2)}$	Port K, L	-10 to 0	mA
	$I_{OP(3)}$	Port M to P	-15 to 0	mA
Average Output Current	$I_{OA(1)}$	Port C to J	-2 to +15	mA
	$I_{OA(2)}$	Port K, L	-10 to 0	mA
	$I_{OA(3)}$	Port M to P	-15 to 0	mA
	$\Sigma I_{OA(1)}$	Total current of all pins (Note 2)	Port C, D, E	-30 to +50
	$\Sigma I_{OA(2)}$	Total current of all pins (Note 2)	Port F to J	-30 to +50
	$\Sigma I_{OA(3)}$	Total current of all pins (Note 2)	Port K, L, M	-50 to 0
	$\Sigma I_{OA(4)}$	Total current of all pins (Note 2)	Port N, O, P	-50 to 0
Allowable Power Dissipation	$P_d\text{ max(1)}$	$T_a=-30$ to $+70^{\circ}\text{C}$ (QIP)	430	mW
	$P_d\text{ max(2)}$	$T_a=-30$ to $+70^{\circ}\text{C}$ (DIP)	600	mW
Operating Temperature	T_{opr}		-30 to +70	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

2. Allowable Operating Conditions/ $T_a=-30$ to $+70^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $V_{DD}=4.0$ to 5.5V

			min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.0	5.5	V
Standby Supply Voltage	V_{st}	RAM, register hold (Note 3)	V_{DD}	1.8	5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$	Port A, B ₀ to 2	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of OD type (Port C to J)	$0.7V_{DD}$	+13.5	V
	$V_{IH(3)}$	Output Nch Tr OFF	Port of PU type (Port C to J)	$0.7V_{DD}$	V_{DD}	V
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{\text{INT}}, \overline{\text{SCK}}, \text{SI}$ of OD type	$0.8V_{DD}$	+13.5	V
	$V_{IH(5)}$	Output Nch Tr OFF	$\overline{\text{INT}}, \overline{\text{SCK}}, \text{SI}$ of PU type	$0.8V_{DD}$	V_{DD}	V
	$V_{IH(6)}$		$\overline{\text{RES}}$	$0.8V_{DD}$	V_{DD}	V
	$V_{IH(7)}$	External clock mode	OSC1	$0.8V_{DD}$	V_{DD}	V
	$V_{IH(8)}$	Fig. 8	High V_t input circuit of Port B ₃	$V_{DD}-0.5$	+13.5	V
	$V_{IH(9)}$	Fig. 8	Low V_t input circuit of Port B ₃	$0.5V_{DD}$	+13.5	V

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LC6554D

				min	typ	max	unit
“L”-Level Input Voltage	V _{IL} (1)	Port A, B ₀ to 2	V _{SS}		+0.5	V	
	V _{IL} (2)	Port C to J	V _{SS}		0.3V _{DD}	V	
	V _{IL} (3)	INT, SCK, SI	V _{SS}		0.25V _{DD}	V	
	V _{IL} (4)	TEST	V _{SS}		0.3V _{DD}	V	
	V _{IL} (5)	RES	V _{SS}		0.25V _{DD}	V	
	V _{IL} (6)	External clock mode	OSC1	V _{SS}	0.25V _{DD}	V	
	V _{IL} (7)	Fig. 8	Low V _t input circuit of Port B ₃	V _{SS}		+0.9	V
See Table 2.							
Operating Frequency (Cycle Time)	f _{op} (T _{CYC})			384 (10.4)		1444 (2.77)	kHz (μs)
External Clock Conditions (When the external clock or 2-pin RC OSC option is selected)							
Frequency	f _{ext}	Fig. 1	OSC1		See Table 2.		
Pulse Width	textH, textL		OSC1	90		ns	
Rise/Fall Time	textR, textF		OSC1		30	ns	
Oscillation Guaranteed Constants							
2-Pin RC Oscillation	C _{ext}	Fig. 2	OSC1, OSC2		220±5%		pF
	R _{ext}	Fig. 2	OSC1, OSC2		6.8±1%		kΩ
Ceramic Resonator Oscillation		Fig. 3			See Table 1.		
3. Electrical Characteristics/T _a =−30 to +70°C, V _{SS} =0V, V _{DD} =4.0 to 5.5V							
“H”-Level Input Current	I _{IH} (1)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V _{IN} =+13.5V	Port of OD type (Port C to J) Port A, B			+5.0	μA
	I _{IH} (2)	External clock mode, V _{IN} =V _{DD}	OSC1			+1.0	μA
“L”-Level Input Current	I _{IL} (1)	Output Nch Tr OFF V _{IN} =V _{SS}	Port of OD type (Port C to J) Port A, B	−1.0			μA
	I _{IL} (2)	Output Nch Tr OFF V _{IN} =V _{SS}	Port of PU type (Port C to J)	−1.3	−0.35		mA
	I _{IL} (3)	V _{IN} =V _{SS}	RES	−45	−10		μA
	I _{IL} (4)	External clock mode, V _{IN} =V _{SS}	OSC1	−1.0			μA
“H”-Level Output Voltage	V _{OH} (1)	I _{OH} =−50μA	Port of PU type (Port C to J)	V _{DD} −1.2			V
	V _{OH} (2)	I _{OH} =−3mA	Port K, L	V _{DD} −1.8			V
	V _{OH} (3)	I _{OH} =−10mA	Port M to P	V _{DD} −1.8			V
“L”-Level Output Voltage	V _{OL} (1)	I _{OL} =10mA	Port C to J			1.5	V
	V _{OL} (2)	I _{OL} =2mA, When I _{OL} of each port is 2mA or less	Port C to J			0.5	V
	V _{OL} (3)	Output Pch Tr OFF V _p =−35V Output open	Port of PD type (Port K to P)			−33	V
Output OFF Leakage Current	I _{OFF} (1)	Output Pch Tr OFF V _{OUT} =V _{DD}	Port of OD type (Port K to P)			+30	μA
	I _{OFF} (2)	Output Pch Tr OFF V _{OUT} =V _{DD} −40V	Port of OD type (Port K to P)	−30			μA
Hysteresis Voltage	V _{HYS}		RES, INT, SCK, SI, OSC1 of Schmitt type (Note 5)	0.1V _{DD}			V

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LC6554D

					min	typ	max	unt
Current Dissipation								
Operation mode, Output Nch Tr, Pch Tr OFF, Port=V _{DD}								
2-Pin RC Oscillation Mode	I _{DDOP} (1)	Fig. 2 f _{OSC} =700kHz(TYP)	V _{DD}			1.5	5	mA
Ceramic Resonator	I _{DDOP} (2)	Fig. 3 4MHz, 1/3 predivider	V _{DD}			5	10	mA
Oscillation Mode	I _{DDOP} (3)	Fig. 3 4MHz, 1/4 predivider	V _{DD}			5	10	mA
	I _{DDOP} (4)	Fig. 3 3MHz, 1/3 predivider	V _{DD}			4	9	mA
	I _{DDOP} (5)	Fig. 3 3MHz, 1/4 predivider	V _{DD}			4	9	mA
	I _{DDOP} (6)	Fig. 3 400kHz	V _{DD}			0.6	3	mA
	I _{DDOP} (7)	Fig. 3 800kHz*	V _{DD}			1.2	4	mA
External Clock Mode	I _{DDOP} (8)	384kHz to 1444kHz,	V _{DD}			2	6	mA
		1/1 predivider						
		1152kHz to 4330kHz,	V _{DD}			5	10	mA
Standby Mode	I _{DDSt}	1/3 predivider						
		1536kHz to 4330kHz,						
		1/4 predivider						
		V _{DD} =5.5V	V _{DD}			0.05	10	μA
Oscillation Characteristics								
Ceramic Resonator Oscillation								
Oscillation Frequency	f _{COSC} (Note 4)	Fig. 3 fo=400kHz	OSC1, OSC2	392	400	408	kHz	
		Fig. 3 fo=800kHz	OSC1, OSC2	784	800	816	kHz	
		Fig. 3 fo=3MHz,	OSC1, OSC2	2940	3000	3060	kHz	
		1/3 predivider						
		1/4 predivider						
		Fig. 3 fo=4MHz,	OSC1, OSC2	3920	4000	4080	kHz	
		1/3 predivider						
		1/4 predivider						
Oscillation Stabilizing Period	t _{CFS}	Fig. 4 fo=400kHz, 800kHz, 3MHz, 4MHz					10	ms
2-Pin RC Oscillation								
Oscillation Frequency	f _{MOSC}	Fig. 2 C _{ext} =220pF ±5% R _{ext} =6.8kΩ ±1%	OSC1, OSC2	486	700	1056	kHz	
Pull-up Resistance								
I/O Port Pull-up Resistance	R _{pp}	V _{DD} =5V	Port of PU type (Port C to J)		14			kΩ
Pull-down Resistance								
Output Port Pull-down Resistance	R _{pd}	V _{DD} =5V	Port of PD type (Port K to P)	50		200		kΩ
External Reset Characteristics								
Reset Time	T _{RST}				See Fig. 5.			

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LC6554D

Pin Capacitance	CP	f=1MHz Other than pins to be tested, V _{IN} =V _{SS}		min	typ 10	max	unit pF
Serial Clock							
Input Clock Cycle Time	t _{CKCY} (1)	Fig. 6	$\overline{\text{SCK}}$	3.0			μs
Output Clock Cycle Time	t _{CKCY} (2)	Fig. 6	$\overline{\text{SCK}}$		64 × T _{CYC} (T _{CYC} =4 × System clock period)		μs
Input Clock "L"-Level Pulse Width	t _{CKL} (1)	Fig. 6	$\overline{\text{SCK}}$	1.0			μs
Output Clock "L"-Level Pulse Width	t _{CKL} (2)	Fig. 6	$\overline{\text{SCK}}$		32 × T _{CYC}		μs
Input Clock "H"-Level Pulse Width	t _{CKH} (1)	Fig. 6	$\overline{\text{SCK}}$	1.0			μs
Output Clock "H"-Level Pulse Width	t _{CKH} (2)	Fig. 6	$\overline{\text{SCK}}$		32 × T _{CYC}		μs
Serial Input							
Data Setup Time	t _{ICK}	Specified for ↑ of $\overline{\text{SCK}}$, Fig. 6	SI	0.5			μs
Data Hold Time	t _{CKI}		SI	0.5			μs
Serial Output							
Output Delay Time	t _{CKO}	Specified for ↓ of $\overline{\text{SCK}}$, Nch OD only: External 1kohm, external 50pF Fig. 6	SO			0.5	μs
Pulse Output							
Period	t _{PCY}	Fig. 7	PE ₀		64 × T _{CYC}		μs
"H"-Level Pulse Width	t _{PH}	T _{CYC} =4 × System clock period, Nch OD only:	PE ₀		32 × T _{CYC} ±10%		μs
"L"-Level Pulse Width	t _{PL}	External 1kohm, external 50pF	PE ₀		32 × T _{CYC} ±10%		μs

Note 1: When oscillated internally under the oscillating conditions in Fig. 3, up to the oscillation amplitude generated is allowable.

Note 2: Average over the period of 100msec.

Note 3: Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.

The PB₃ pin must be free from chattering during the HALT instruction execution cycle.

Note 4: f_{COSC} represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

Note 5: The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

Note 6: When mounting the QIP version on the board, do not dip it in solder.

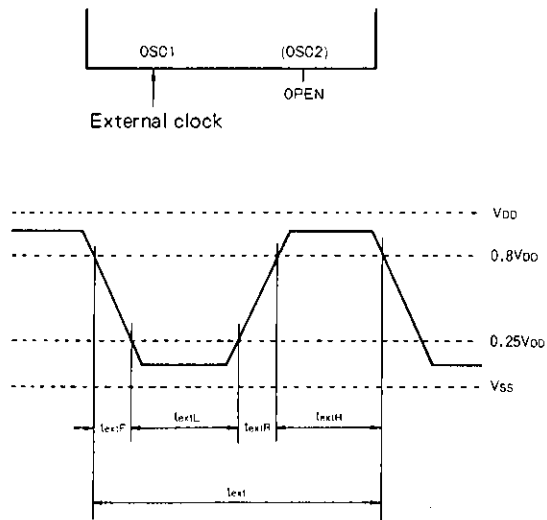


Fig. 1 External Clock Input Waveform

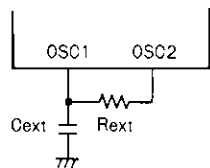


Fig. 2 2-Pin RC Oscillation Circuit

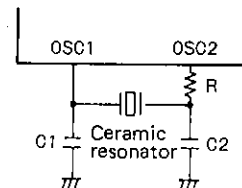


Fig. 3 Ceramic Resonator Oscillation Circuit

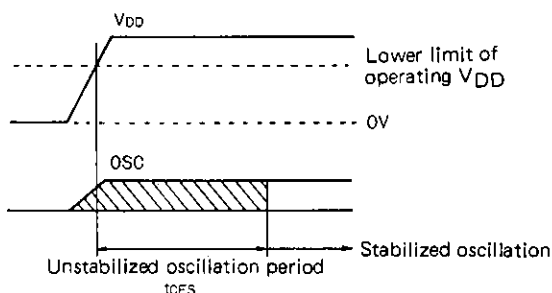


Fig. 4 Oscillation Stabilizing Period

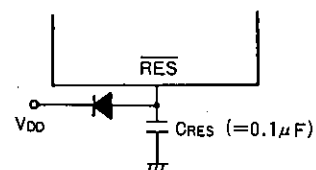


Fig. 5 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at $C_{RES}=0.1\mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10 ms or greater.

4MHz CSA4.00MG (Murata)	C 1	33pF±10%	800KHz CSB800D CSB800K (Murata)	C 1	220pF±10%
	C 2	33pF±10%		C 2	220pF±10%
	R	0Ω		R	0Ω
4MHz KBR4.0MS (Kyocera)	C 1	33pF±10%	800KHz KBR800H (Kyocera)	C 1	220pF±10%
	C 2	33pF±10%		C 2	220pF±10%
	R	0Ω		R	0Ω
3MHz CSA3.00MG (Murata)	C 1	33pF±10%	400KHz CSB400P (Murata)	C 1	330pF±10%
	C 2	33pF±10%		C 2	330pF±10%
	R	0Ω		R	0Ω
3MHz KBR3.0MS (Kyocera)	C 1	47pF±10%	400KHz KBR400B (Kyocera)	C 1	330pF±10%
	C 2	47pF±10%		C 2	330pF±10%
	R	0Ω		R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

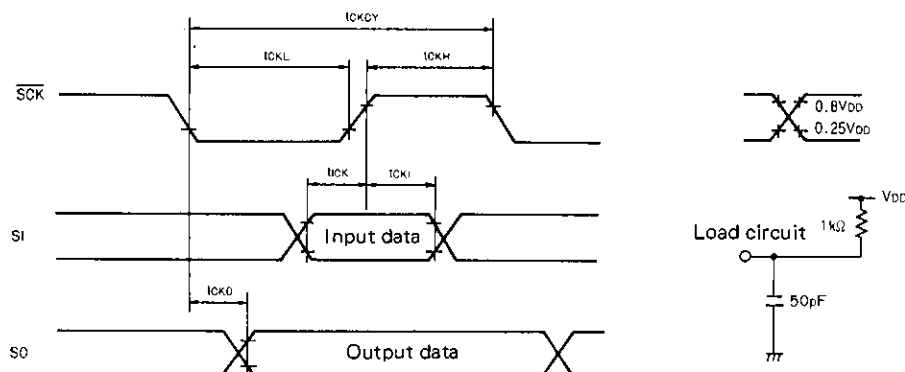
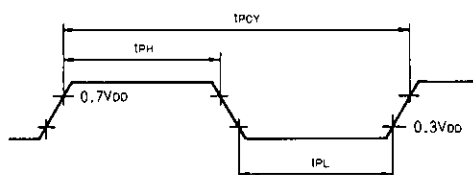


Fig. 6 Serial Input/Output Timing



The load conditions are the same as in Fig. 6.

Fig. 7 Pulse Output Timing at Port PE0

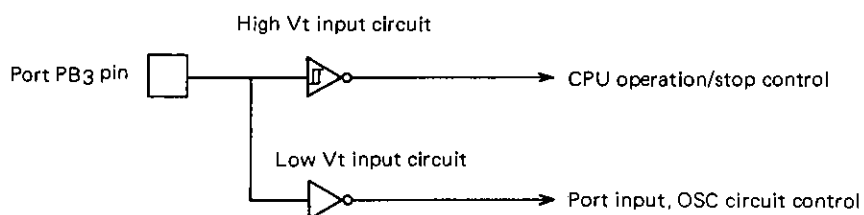


Fig. 8 Port PB3 High Vt/Low Vt Input Circuit

Table 2 LC6554D

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.) $V_{DD}=4$ to 5.5V

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator Option	400 kHz	1/1 (10 μ s)	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 μ s)	Unusable with 1/3, 1/4 predivider
	3 MHz	1/3 (4 μ s) 1/4 (5.33 μ s)	Unusable with 1/1 predivider
	4 MHz	1/3 (3 μ s) 1/4 (4 μ s)	Unusable with 1/1 predivider
External Clock Option or External Clock Drive by RC OSC Option	384 to 1444 kHz 1152 to 4330 kHz 1536 to 4330 kHz	1/1 (10.4 to 2.77 μ s) 1/3 (10.4 to 2.77 μ s) 1/4 (10.4 to 3.70 μ s)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option or RC OSC option.		
RC OSC Option	Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the predivider option, frequency, V_{DD} range must be the same as for the external clock option.		

RC Oscillation Characteristic of the LC6554D

Fig. 8 shows the RC oscillation characteristic of the LC6554D. For the variation range of RC OSC frequency of the LC6554D, the following are guaranteed at the external constants only shown below.

External constants $C_{ext}=220$ pF, $R_{ext}=6.8$ kohms

$486 \text{ kHz} \leq f_{MOSC} \leq 1056 \text{ kHz}$ ($T_a=-30^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD}=4.0$ to 5.5 V)

If any other constants than specified above are used, the range of $R_{ext} = 4$ kohms to 20 kohms, $C_{ext} = 150$ pF to 390 pF must be observed. (See Fig. 8.)

Note 8: The oscillation frequency at $V_{DD}=5.0$ V, $T_a=25^\circ\text{C}$ must not exceed 700 kHz.

Note 9: The oscillation frequency at $V_{DD}=4$ to 5.5 V, $T_a=-30$ to $+70^\circ\text{C}$ must be within the operation clock frequency range (384 kHz to 1444 kHz).

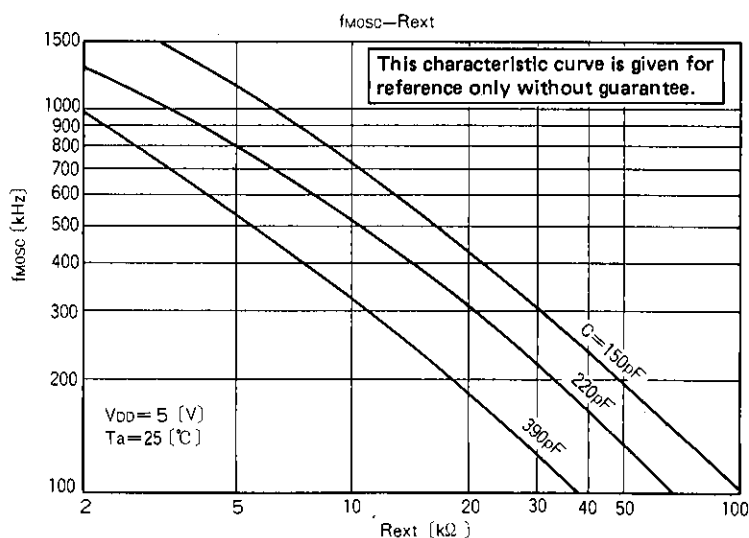


Fig. 8 RC Oscillation Frequency Data (Typ.)

LC6554H

1. Absolute Maximum Ratings/ $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

Maximum Supply Voltage	$V_{DD\text{ max}}$	V_{DD}	−0.3 to +7.0	unit
Output Voltage	$V_{O(1)}$	OSC2	Allowable up to voltage generated	V
	$V_{O(2)}$	Port K to P	$V_{DD}-45$ to $V_{DD}+0.3$	V
Input Voltage	$V_{I(1)}$	OSC1 (Note 1)	−0.3 to $V_{DD}+0.3$	V
	$V_{I(2)}$	TEST, RES	−0.3 to $V_{DD}+0.3$	V
	$V_{I(3)}$	Port A, B	−0.3 to +15	V
	$V_{I(4)}$	Vp	$V_{DD}-45$ to $V_{DD}+0.3$	V
Input/Output Voltage	$V_{IO(1)}$	Port of OD type (Port C to J)	−0.3 to +15	V
	$V_{IO(2)}$	Port of PU type (Port C to J)	−0.3 to $V_{DD}+0.3$	V
Peak Output Current	$I_{OP(1)}$	Port C to J	−2 to +15	mA
	$I_{OP(2)}$	Port K, L	−10 to 0	mA
	$I_{OP(3)}$	Port M to P	−15 to 0	mA
Average Output Current	$I_{OA(1)}$	Per pin over the period of 100 msec. Port C to J	−2 to +15	mA
	$I_{OA(2)}$	Per pin over the period of 100 msec. Port K, L	−10 to 0	mA
	$I_{OA(3)}$	Per pin over the period of 100 msec. Port M to P	−15 to 0	mA
	$\Sigma I_{OA(1)}$	Total current of all pins (Note 2) Port C, D, E	−30 to +50	mA
	$\Sigma I_{OA(2)}$	Total current of all pins (Note 2) Port F to J	−30 to +50	mA
	$\Sigma I_{OA(3)}$	Total current of all pins (Note 2) Port K, L, M	−50 to 0	mA
	$\Sigma I_{OA(4)}$	Total current of all pins (Note 2) Port N, O, P	−50 to 0	mA
Allowable Power Dissipation	$P_{d\text{ max}(1)}$	$T_a=-30$ to $+70^{\circ}\text{C}$ (QIP)	430	mW
	$P_{d\text{ max}(2)}$	$T_a=-30$ to $+70^{\circ}\text{C}$ (DIP)	600	mW
Operating Temperature	T_{opr}		−30 to +70	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		−55 to +125	$^{\circ}\text{C}$

2. Allowable Operating Conditions/ $T_a=-30$ to $+70^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $V_{DD}=4.5$ to 5.5V

			min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.5	5.5	V
Standby Supply Voltage	V_{st}	RAM, register hold(Note 3)	V_{DD}	1.8	5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$	Port A, B ₀ to 2	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of OD type (Port C to J)	$0.7V_{DD}$	+13.5	V
	$V_{IH(3)}$	Output Nch Tr OFF	Port of PU type (Port C to J)	$0.7V_{DD}$	V_{DD}	V
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI of OD type	$0.8V_{DD}$	+13.5	V
	$V_{IH(5)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI of PU type	$0.8V_{DD}$	V_{DD}	V
	$V_{IH(6)}$		$\overline{RES}$	$0.8V_{DD}$	V_{DD}	V
	$V_{IH(7)}$	External clock mode	OSC1	$0.8V_{DD}$	V_{DD}	V
	$V_{IH(8)}$	Fig. 7	High Vt input circuit of Port B ₃	$V_{DD}-0.5$	+13.5	V
	$V_{IH(9)}$	Fig. 7	Low Vt input circuit of Port B ₃	$0.5V_{DD}$	+13.5	V

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LC6554H

			min	typ	max	unit
“L”-Level Input Voltage	V _{IL} (1)	Port A, B ₀ to 2	V _{SS}		+0.5	V
	V _{IL} (2)	Port C to J	V _{SS}	0.3V _{DD}		V
	V _{IL} (3)	$\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI	V _{SS}	0.25V _{DD}		V
	V _{IL} (4)	TEST	V _{SS}	0.3V _{DD}		V
	V _{IL} (5)	$\overline{\text{RES}}$	V _{SS}	0.25V _{DD}		V
	V _{IL} (6)	External clock mode	OSC1	V _{SS}	0.25V _{DD}	V
	V _{IL} (7)	Fig. 7	Low V _t input circuit of Port B ₃	V _{SS}	+0.9	V
See Table 2.						
Operating Frequency (Cycle Time)	f _{op} (T _{CYC})		384 (10.4)		4330 (0.92)	kHz (μs)
External Clock Conditions (When the external clock option is selected)						
Frequency	f _{ext}	Fig. 1	OSC1	See Table 2.		
Pulse Width	textH, textL		OSC1	90		ns
Rise/Fall Time	textR, textF		OSC1		30	ns
Oscillation Guaranteed Constants						
Ceramic Resonator Oscillation	Fig. 2		See Table 1.			
3. Electrical Characteristics/T_a=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 5.5V						
			min	typ	max	unit
“H”-Level Input Current	I _{IH} (1)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V _{IN} =+13.5V	Port of OD type (Port C to J) Port A, B		+5.0	μA
	I _{IH} (2)	External clock mode, V _{IN} =V _{DD}	OSC1		+1.0	μA
“L”-Level Input Current	I _{IL} (1)	Output Nch Tr OFF V _{IN} =V _{SS}	Port of OD type (Port C to J) Port A, B	−1.0		μA
	I _{IL} (2)	Output Nch Tr OFF V _{IN} =V _{SS}	Port of PU type (Port C to J)	−1.3	−0.35	mA
	I _{IL} (3)	V _{IN} =V _{SS}	$\overline{\text{RES}}$	−45	−10	μA
	I _{IL} (4)	External clock mode, V _{IN} =V _{SS}	OSC1	−1.0		μA
“H”-Level Output Voltage	V _{OH} (1)	I _{OH} =−50μA	Port of PU type (Port C to J)	V _{DD} −1.2		V
	V _{OH} (2)	I _{OH} =−3mA	Port K, L	V _{DD} −1.8		V
	V _{OH} (3)	I _{OH} =−10mA	Port M to P	V _{DD} −1.8		V
“L”-Level Output Voltage	V _{OL} (1)	I _{OL} =10mA	Port C to J		1.5	V
	V _{OL} (2)	I _{OL} =2mA, When I _{OL} of each port is 2mA or less	Port C to J		0.5	V
	V _{OL} (3)	Output Pch Tr OFF V _p =−35V Output open	Port of PD type (Port K to P)		−33	V
Output OFF Leakage Current	I _{OFF} (1)	Output Pch Tr OFF V _{OUT} =V _{DD}	Port of OD type (Port K to P)		+30	μA
	I _{OFF} (2)	Output Pch Tr OFF V _{OUT} =V _{DD} −40V	Port of OD type (Port K to P)	−30		μA
Hysteresis Voltage	V _{HYS}		$\overline{\text{RES}}$, $\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI, OSC1 of Schmitt type (Note 5)	0.1V _{DD}		V

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LC6554H

				min	typ	max	unit
Current Dissipation							
Ceramic Resonator Oscillation Mode	$I_{DDOP(1)}$	Fig. 2 4MHz	VDD Operating mode, Output Nch Tr, Pch Tr OFF, Port = VDD		5	10	mA
External Clock Mode	$I_{DDOP(2)}$	384 kHz to 4330 kHz			5	10	mA
Standby Mode	I_{DDST}	Output Nch Tr OFF		VDD	0.05	10	μ A
		Output Pch Tr OFF		VDD			
		Port VDD, VDD=5.5 V					
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC} (Note 4)	Fig. 2 $f_0=4$ MHz	OSC1, OSC2	3920	4000	4080	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 3 $f_0=4$ MHz				10	ms
Pull-up Resistance							
I/O Port Pull-up Resistance	R_{pp}	$V_{DD}=5V$	Port of PU type (Port C to J)		14		k Ω
Pull-down Resistance							
Output Port Pull-down Resistance	R_{pd}	$V_{DD}=5V$	Port of PD type (Port K to P)	50		200	k Ω
External Reset Characteristics							
Reset Time	T_{RST}				See Fig. 4.		

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LC6554H

Pin Capacitance	CP	f=1MHz Other than pins to be tested, V _{IN} =V _{SS}		min	typ 10	max	unit
Serial Clock							
Input Clock Cycle Time	t _{CKCY} (1)	Fig. 5	$\overline{\text{SCK}}$	3.0			μs
Output Clock Cycle Time	t _{CKCY} (2)	Fig. 5	$\overline{\text{SCK}}$		64 × T _{CYC}		μs
(T _{CYC} =4 × System clock period)							
Input Clock "L"-Level Pulse Width	t _{CKL} (1)	Fig. 5	$\overline{\text{SCK}}$	1.0			μs
Output Clock "L"-Level Pulse Width	t _{CKL} (2)	Fig. 5	$\overline{\text{SCK}}$		32 × T _{CYC}		μs
Input Clock "H"-Level Pulse Width	t _{CKH} (1)	Fig. 5	$\overline{\text{SCK}}$	1.0			μs
Output Clock "H"-Level Pulse Width	t _{CKH} (2)	Fig. 5	$\overline{\text{SCK}}$		32 × T _{CYC}		μs
Serial Input							
Data Setup Time	t _{ICK}	Specified for ↑ of $\overline{\text{SCK}}$, Fig. 5	SI	0.5			μs
Data Hold Time	t _{CKI}		SI	0.5			μs
Serial Output							
Output Delay Time	t _{CKO}	Specified for ↓ of $\overline{\text{SCK}}$, Nch OD only: External 1kohm, external 50pF Fig. 5	SO			0.5	μs
Pulse Output							
Period	t _{PCY}	Fig. 6	PE ₀		64 × T _{CYC}		μs
"H"-Level Pulse Width	t _{PH}	T _{CYC} =4 × System clock period, Nch OD only:	PE ₀		32 × T _{CYC} ±10%		μs
"L"-Level Pulse Width	t _{PL}	External 1kohm, external 50pF	PE ₀		32 × T _{CYC} ±10%		μs

Note 1: When oscillated internally under the oscillating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.

Note 2: Average over the period of 100ms.

Note 3: Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.

The PB₃ pin must be free from chattering during the HALT instruction execution cycle.

Note 4: f_{CFOSC} represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

Note 5: The OSC1 becomes the Schmitt type when the OSC option is the external clock OSC.

Note 6: When mounting the QIP version on the board, do not dip it in solder.

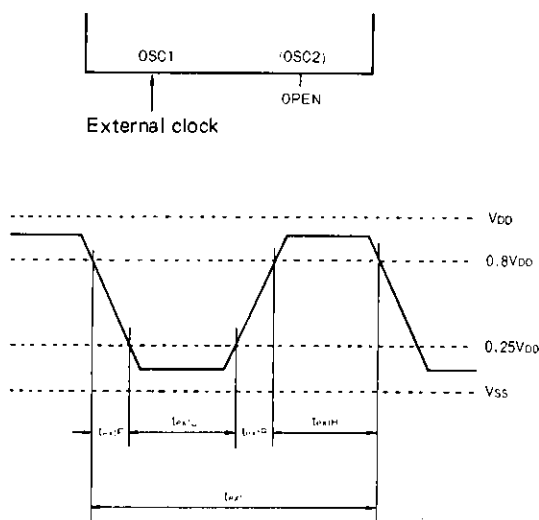


Fig. 1 External Clock Input Waveform

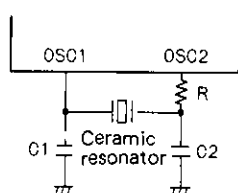


Fig. 2 Ceramic Resonator Oscillation Circuit

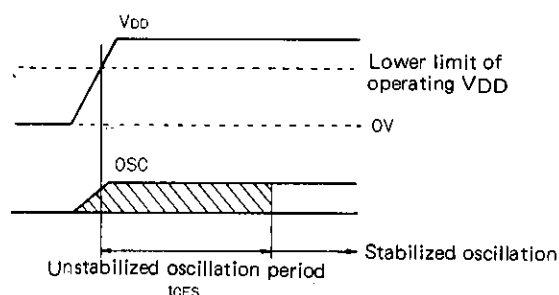


Fig. 3 Oscillation Stabilizing Period

4MHz CSA4.00MG (Murata)	C 1	33pF±10%
	C 2	33pF±10%
	R	0Ω
4MHz KBR4.0MS (Kyocera)	C 1	33pF±10%
	C 2	33pF±10%
	R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

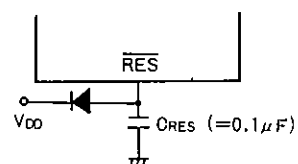


Fig. 4 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100ms at $C_{RES}=0.1\mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or greater.

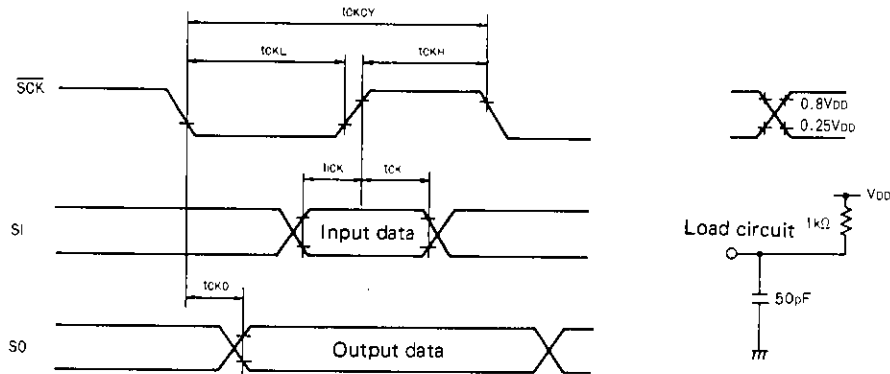
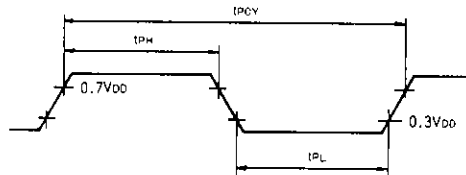


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port PE0

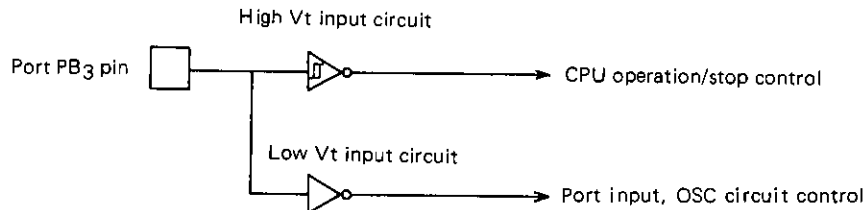


Fig. 7 Port PB3 High Vt/Low Vt Input Circuit

Table 2 LC6554H

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.) $V_{DD}=4.5$ to $5.5V$

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator OSC Option	4 MHz	1/1 (1 μs)	
External Clock Option	384 to 4330 kHz	1/1 (10.4 to 0.92 μs)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option.		

LC6554D/H INSTRUCTION SET

Symbol	Description				
AC	: Accumulator	M(DP)	: Memory addressed by DP	{ }, []	: Contents
ACt	: Accumulator bit t	P(DP _L)	: Input/output port addressed by DP _L	←	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
CTL	: Control register	STACK	: Stack register	−	: Subtraction
DP	: Data pointer	TM	: Timer	^	: AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨	: OR
EXTF	: External interrupt request flag	At, Ha, La	: Working register	⊙	: Exclusive OR
Fn	: Flag bit n	ZF	: Zero flag		
M	: Memory				

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← (AC)	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ₀ ← (CF), AC _{n-1} ← (AC _n), CF ← (AC ₃)	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← (M(DP)) + 1	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← (M(DP)) - 1	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B ₁ B ₀	1	1	M(DP, B ₁ B ₀) ← 1		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B ₁ B ₀	1	1	M(DP, B ₁ B ₀) ← 0	ZF	
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) v (M(DP))	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ^ (M(DP))	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) v (M(DP))	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	(M(DP)) + (AC) + 1	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 1 2 1 1 0	2	2	($\overline{I_3 I_2 I_1 I_0}$) + (AC) + 1	ZF CF	
	CLI data	Compare DP _L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 3 1 2 1 1 0	2	2	(DP _L) v ($\overline{I_3 I_2 I_1 I_0}$)	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	1 3 1 2 1 1 0	1	1	AC ← $\overline{I_3 I_2 I_1 I_0}$	ZF	* 1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	ZF	
	XM data	Exchange AC with M, then modify DP _H with immediate data	1 0 1 0	0 M ₂ M ₁ M ₀	2	2	(AC) ↔ (M(DP)) DP _H ← (DP _H) v (OM ₂ M ₁ M ₀)	ZF	The ZF is set/reset according to the result of (DP _H) v (OM ₂ M ₁ M ₀)
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ (M(DP))	ZF	The ZF is set/reset according to the DP _H contents at the time of instruction execution.
	XI	Exchange AC with M, then increment DP _L	1 1 1 1	1 1 1 0	1	2	(AC) ↔ (M(DP)) DP _L ← (DP _L) + 1	ZF	The ZF is set/reset according to the result of (DP _L + 1).
	XD	Exchange AC with M, then decrement DP _L	1 1 1 1	1 1 1 1	1	2	(AC) ↔ (M(DP)) DP _L ← (DP _L) - 1	ZF	The ZF is set/reset according to the result of (DP _L - 1).
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PC, E, AC)		

LC6554D, 6554H

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Data pointer manipulation instructions	LDZ data	Load DP _H with Zero and DP _L with immediate data respectively	1 0 0 0 1 3 2 1 1 0	1	1	DP _H ← 0 DP _L ← 1 3 2 1 1 0	The DP _H and DP _L are loaded with 0 and the immediate data 1 3 2 1 1 0 respectively.		
	LHI data	Load DP _H with immediate data	0 1 0 0 1 3 2 1 1 0	1	1	DP _H ← 1 3 2 1 1 0	The DP _H is loaded with the immediate data 1 3 2 1 1 0.		
	IND	Increment DP _L	1 1 1 0 1 1 1 0	1	1	DP _L ← (DP _L) + 1	The DP _L contents are incremented +1.	ZF	
	DED	Decrement DP _L	1 1 1 0 1 1 1 1	1	1	DP _L ← (DP _L) - 1	The DP _L contents are decremented -1.	ZF	
	TAL	Transfer AC to DP _L	1 1 1 1 0 1 1 1	1	1	DP _L ← (AC)	The AC contents are transferred to the DP _L		
	TLA	Transfer DP _L to AC	1 1 1 1 0 1 0 1	1	1	AC ← (DP _L)	The DP _L contents are transferred to the AC	ZF	
	XAH	Exchange AC with DP _H	0 0 1 0 0 0 1 1	1	1	(AC) ↔ (DP _H)	The AC contents and the DP _H contents are exchanged.		
Working register manipulation instructions	XAI	Exchange AC with working register Ai	1 1 1 0 1 1 1 0	1	1	(AC) ↔ (A ₀)	The AC contents and the contents of working register Ai are exchanged. Ai is assigned one of A ₀ , A ₁ , A ₂ , A ₃ according to t ₁ t ₀ .		
	XAO		1 1 1 0 0 1 1 0	1	1	(AC) ↔ (A ₁)			
	XAI		1 1 1 0 1 1 0 0	1	1	(AC) ↔ (A ₂)			
	XA3		1 1 1 0 1 1 0 0	1	1	(AC) ↔ (A ₃)			
	XHa	Exchange DP _H with working register Ha	1 1 1 1 1 1 1 0	1	1	(DP _H) ↔ (H ₀)	The DP _H contents and the contents of working register Ha are exchanged. Ha is assigned either of H ₀ or H ₁ according to a.		
	XH1		1 1 1 1 1 1 0 0	1	1	(DP _H) ↔ (H ₁)			
Flag manipulation instructions	XLa	Exchange DP _L with working register La	1 1 1 1 0 1 1 0	1	1	(DP _L) ↔ (L ₀)	The DP _L contents and the contents of working register La are exchanged. La is assigned either of L ₀ or L ₁ according to a.		
	XL1		1 1 1 1 0 1 0 0	1	1	(DP _L) ↔ (L ₁)			
	SFB flag	Set flag bit	0 1 0 1 B ₃ B ₂ B ₁ B ₀	1	1	F _n ← 1	The flag specified with B ₃ B ₂ B ₁ B ₀ is set.		
	RFB flag	Reset flag bit	0 0 0 1 B ₃ B ₂ B ₁ B ₀	1	1	F _n ← 0	The flag specified with B ₃ B ₂ B ₁ B ₀ is reset.	ZF	The flags are divided into 4 groups of F ₀ to F ₃ , F ₄ to F ₇ , F ₈ to F ₁₁ , F ₁₂ to F ₁₅ . The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B ₃ B ₂ B ₁ B ₀ .
	JMP addr	Jump in the current bank	0 1 1 0 P ₇ P ₆ P ₅ P ₄ 1 P ₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀	2	2	PC ← PC ₁₁ (X) (Z PC ₁₁) P ₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A jump to the address specified with the PC ₁₁ (or PC ₁₁) and immediate data P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ occurs.		If the BANK and JMP instructions are executed consecutively, PC ₁₁ → PC ₁₁ .
	JPEA	Jump in the current page modified by E and AC	1 1 1 1 1 0 1 0	1	1	PC ₇₋₀ ← (E, AC)	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
Jump/subroutine instructions	CZP addr	Call subroutine in the zero page	1 0 0 1 P ₃ P ₂ P ₁ P ₀	1	1	STACK ← (PC) + 1 PC ₁₁₋₈ , PC ₁₋₀ ← 0 PC ₅₋₂ ← P ₃ P ₂ P ₁ P ₀	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 0 1 0 P ₇ P ₆ P ₅ P ₄ 1 P ₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀	2	2	STACK ← (PC) + 2 PC ₁₁₋₅ ← 0 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0 0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0 0 0 1 0	1	1	PC ← (STACK) CF, ZF ← CSF, ZSF	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1 1 1 0 1	1	1	PC ₁₁ ← (PC ₁₁)	The bank is changed.		Effective only when used immediately before the JMP instruction.
	SB	Set bank	0 1 1 0 0 1 1 0	1	1	PC ₁₂ PC ₁₁ ← 1, 10	The bank is changed. Effective only when used immediately before the JMP instruction.		Applicable only to LC6595
Branch instructions	BA _t addr	Branch on AC bit	0 1 1 1 P ₇ P ₆ P ₅ P ₄ 0 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC _t = 1	If a single bit of the AC specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BN _A t addr	Branch on no AC bit	0 0 1 1 P ₇ P ₆ P ₅ P ₄ 0 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC _t = 0	If a single bit of the AC specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BM _t addr	Branch on M bit	0 1 1 1 P ₇ P ₆ P ₅ P ₄ 0 1 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP, t ₁ t ₀)) = 1	If a single bit of the M(DP) specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNM _t addr	Branch on no M bit	0 0 1 1 P ₇ P ₆ P ₅ P ₄ 0 1 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP, t ₁ t ₀)) = 0	If a single bit of the M(DP) specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BP _t addr	Branch on Port bit	0 1 1 1 P ₇ P ₆ P ₅ P ₄ 1 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP, t ₁ t ₀)) = 1	If a single bit of port P(DP) specified with the immediate data t ₁ t ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNP _t addr	Branch on no Port bit	0 0 1 1 P ₇ P ₆ P ₅ P ₄ 1 0 t ₁ t ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP, t ₁ t ₀)) = 0	If a single bit of port P(DP) specified with the immediate data t ₁ t ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.

LC6554D, 6554H

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Branch instructions	BTM addr	Branch on timer	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The TMF is reset.	TMF
	BNTM addr	Branch on no timer	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The TMF is reset.	TMF
	BI addr	Branch on interrupt	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The EXTF is reset.	EXTF
	BNI addr	Branch on no interrupt	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The EXTF is reset.	EXTF
	BC addr	Branch on CF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.	
	BNC addr	Branch on no CF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.	
	BZ addr	Branch on ZF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.	
	BNZ addr	Branch on no ZF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.	
	BFn addr	Branch on flag bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if F _n = 1	If the flag bit of the 16 flags specified with the immediate data n ₃ n ₂ n ₁ n ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.	Mnemonic is BFO to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC _{7~0} ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if F _n = 0	If the flag bit of the 16 flags specified with the immediate data n ₃ n ₂ n ₁ n ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.	Mnemonic is BNFO to BN15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← {P(DP _L)}	Port P(DP _L) contents are loaded in the AC.	ZF
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP _L) ← {AC}	The AC contents are outputted to port P(DP _L).	
	SPB bit	Set port bit	0 0 0 0	0 1 B ₁ B ₀	1	2	P(DP _L : B ₁ B ₀) ← 1	A single bit in port P(DP _L) specified with the immediate data B ₁ B ₀ is set.	
	RPB bit	Reset port bit	0 0 1 0	0 1 B ₁ B ₀	1	2	P(DP _L : B ₁ B ₀) ← 0	A single bit in port P(DP _L) specified with the immediate data B ₁ B ₀ is reset.	ZF
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL ← {CTL} V B ₃ B ₂ B ₁ B ₀	The bits of the control register specified with the immediate data B ₃ B ₂ B ₁ B ₀ are set.	
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL ← {CTL} A B ₃ B ₂ B ₁ B ₀	The bits of the control register specified with the immediate data B ₃ B ₂ B ₁ B ₀ are reset.	ZF
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← {E} {AC}	The E and AC contents are loaded in the timer. The TMF is reset.	TMF
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.	
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.	

*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, -----, the first CLA instruction only is effective and the following CLA instructions are changed

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