ANALOG DEVICES

AN-316
APPLICATION NOTE

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AD7224 Provides Programmable Voltages Over Varying Ranges

by Mike Byrne

This application note discusses some uses of the AD7224 in providing programmable output voltages over varying ranges. The AD7224 is a monolithic, voltage-mode CMOS DAC with output buffer amplifier housed in a 0.3 inch wide, 18-pin DIP.

The circuit of Figure 1a shows a common configuration for a potentiometer with the output voltage, V_{OUT}, varying from V_A to V_B. This output voltage is varied using the variable resistor VR1. The function performed by this circuit can be implemented using the circuit of Figure 1b. This circuit uses the AD7224 and just three external components to give a programmable output voltage varying from V_X to V_Y.

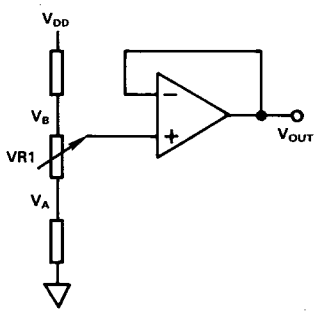

Figure 1a.

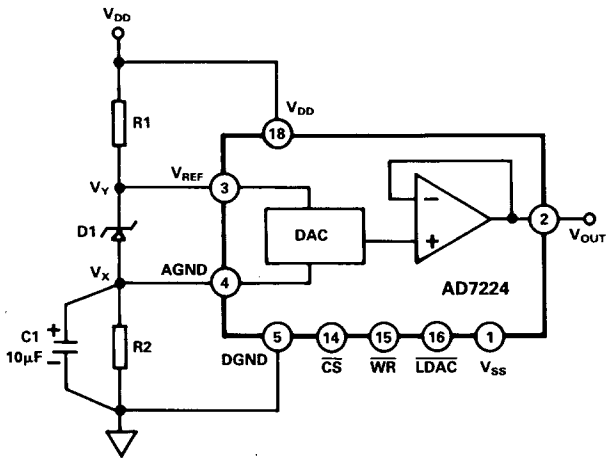

Figure 1b.

The operation of the circuit depends upon the principle that all the current which flows into the V_{REF} input of the AD7224 will flow out of AGND. Therefore, although the current flowing into the V_{REF} input will vary (because of varying input impedance with code) the current flowing through R2 will always remain constant. In practice some current flowing into the V_{REF} input will "leak" away from AGND. This leakage current varies with digital code. This variation is typically of the order of 3µA which represents an error of only 0.05% since the typical current which flows through the zener is 6mA. For example, if V_X is biased at 2V, with R2 = 330Ω the variation of V_X with digital code is typically less than 1mV.

An additional separate current, which does not flow into the V_{REF} input, flows from V_{DD} through internal circuitry and out of AGND. This current is independent of code and therefore does not cause variations in V_X over the input code range. It is in the range 50µA to 150µA and is dependent upon the $(V_Y–V_X)$ voltage; the lower the $(V_Y–V_X)$ voltage the smaller the current. It does mean that V_X, and hence V_Y, will be slightly larger than one would expect based on the current flowing through R1. For example, with R2 = 330Ω, V_{DD} = +12V and $(V_Y–V_X)$ = +6.1V it was found that V_X was 43mV larger than expected. Under the same conditions except $(V_Y–V_X)$ = 3.3V, V_X was 22mV larger than expected. In either case the increased V_X can easily be adjusted for by reducing R2.

The zener diode, D1, must be biased so that the current variation through it will not significantly affect its zener voltage. The worst case variation for the circuit of Figure 1b is 1mA over the input code range but typically this is less than 500µA. The total variation on V_Y, including the effect of the variation on V_X, was found to be less than 2mV. This was for various values of D1 with V_X = 2V and R2 = 330Ω.

The circuit of Figure 1b is not as flexible as that of 1a and a number of limitations exist. V_Y must be at least 4V below the V_{DD} supply voltage to ensure correct operation of the AD7224. Additionally, V_Y must always be positive with respect to V_X and in turn, V_X must always be positive with

respect to DGND. The entire circuit can, however, be operated in single supply with the V_{SS} pin of the AD7224 tied to DGND. When operating in single supply, the AGND should be biased over 2V above DGND to ensure specified linearity performance over the range of reference voltages. This limitation does not apply to differential linearity since the part remains monotonic over the range of reference voltages regardless of whether the part is operated in single or dual supplies. Table I shows different values for R1 and R2 for different zener diode voltages for a V_{DD} supply voltage of +12V. Capacitor C1 is used to eliminate spikes on AGND. These spikes occur when the digital input is changed because the zener diode presents a non-zero impedance to the V_{REF} input. Even without C1 they are not really a problem since they are masked out from the output by the slew rate of the output amplifier.

D1	R1	R2	V_X	V_Y
3.3V	820Ω	390Ω	2.8V	6.28V
3.9V	680Ω	680Ω	4V	8V
4.4V	680Ω	390Ω	2.78V	7.26V
5.6V	680Ω	330Ω	2.16V	7.9V

Table I.

An alternative method for generating a programmable output voltage over a varying range is shown in Figure 2. In this case the AD7224 is used with the LM10, which contains a reference, reference amplifier, A1, and output amplifier, A2, on one chip. The circuit contains just two narrow DIPs and four resistors. The technique involved is one of implicit feedback. For further information on implicit feedback circuits see page 39, "Nonlinear Circuits Handbook" published by Analog Devices.

The on-chip reference on the LM10 is a 200mV reference, V_R. Amplifier A1 is used as a buffer for this reference and has an output current source capability of 1mA. Note that the output voltage from the circuit is taken from the A2 output (which is in fact the reference voltage for the AD7224) and not from the V_{OUT} of the AD7224. The gain placed on amplifier A1 determines the lower end of the output voltage range at V_O. For example, if the gain of this amplifier is 5 the lower end of the V_O range will be 1V while if the gain is unity the lower end will be 200mV. The ratio of R4 and R3 then determines the span of the output voltage. For example, (with a gain of 5 on A1), if R4/R3 = 9 then the output voltage range, at V_O, will be 1V to 10V over the digital input code range of the AD7224. If R4/R3 = 4 then the output voltage range will be 1V to 5V.

The output voltage does not vary in a linear fashion with digital input code. The relationship is shown in Figure 3 for an R4/R3 ratio of 9 and a gain of 5 on A1. The expression for output voltage, V_O, is as follows:

$$V_O = V_R \cdot (1 + G1) \cdot \frac{(1 + G2)}{(1 + G2 \cdot D)}$$

where G1 = R2/R1
G2 = R4/R3

and D is a fractional representation of the digital word in the DAC register ($0 \leq D \leq 255/256$).

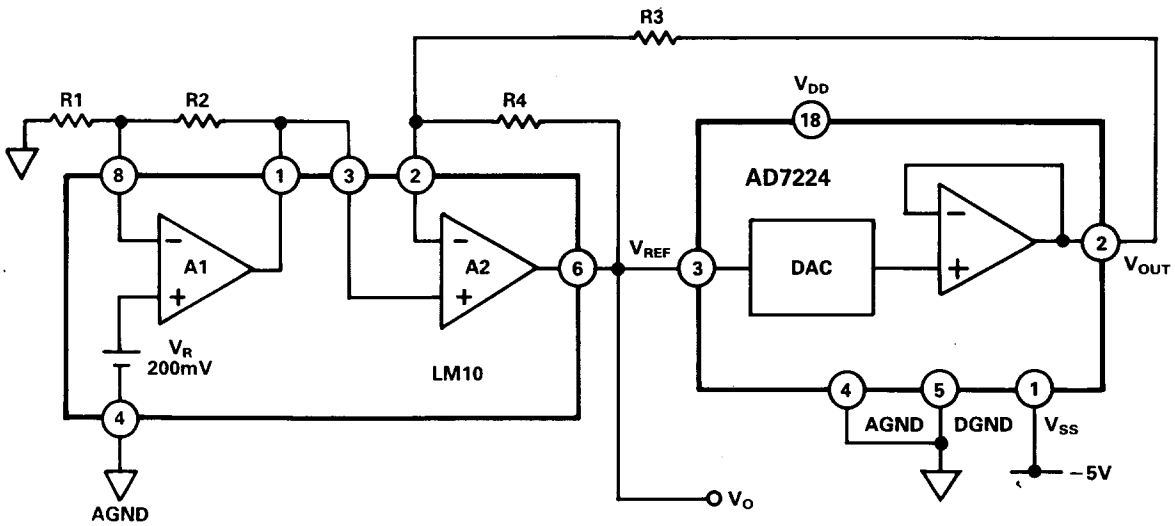

Figure 2. AD7224 with LM10

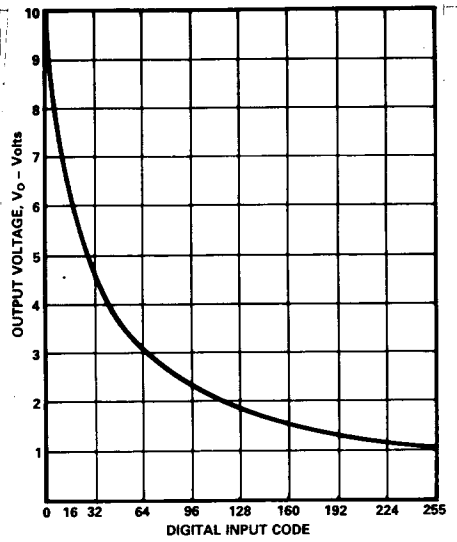

Figure 3. V_O Versus Digital Code

Another configuration, using the AD7224 with the LM10 and giving a similar output voltage range, is outlined in Figure 4. In this case A1 is used to drive the V_{REF} of the AD7224 directly. A2 is then used in conjunction with a series pass transistor, T1, to provide current boosting with up to 100mA being provided across R_L. The output voltage range with the component values given in Figure 4, is, once again, 1V to 10V. The positive supply and return paths for the transistor and load have to be kept separate from the supply paths for the rest of the circuit to avoid errors caused by resistive drops with large currents flowing. Varying the ratios of R6 to R5 and R8 to R7 changes the output voltage range with the expression for the output voltage, V_O, being

$$V_O = V_R \cdot \frac{(1 + G1)\cdot(1 + G2)}{(1 + G1\cdot D)}$$

where G1 = R6/R5
G2 = R8/R7

and D is a fractional representation of the digital word in the DAC register.

In both the circuit of Figure 2 and Figure 4 the AD7224 is shown operating from dual supplies (i.e., $V_{SS} = -5V$). The reason for this is that the AD7224 loses its output sink capability with output voltages near AGND when operated in single supply. In dual supply operation it maintains a 400μA output sink capability over the entire output voltage range. Resistor values for R3 in Figure 2 and R5 in Figure 4 should be chosen so that this 400μA output sink current is not exceeded. If single supply operation is required, the V_{SS} of the AD7224 can be tied to DGND with the AGND of the AD7224 (and all other AGND points in the circuit) biased to 2V. In this case the output will again have its full sink capability over the output range.

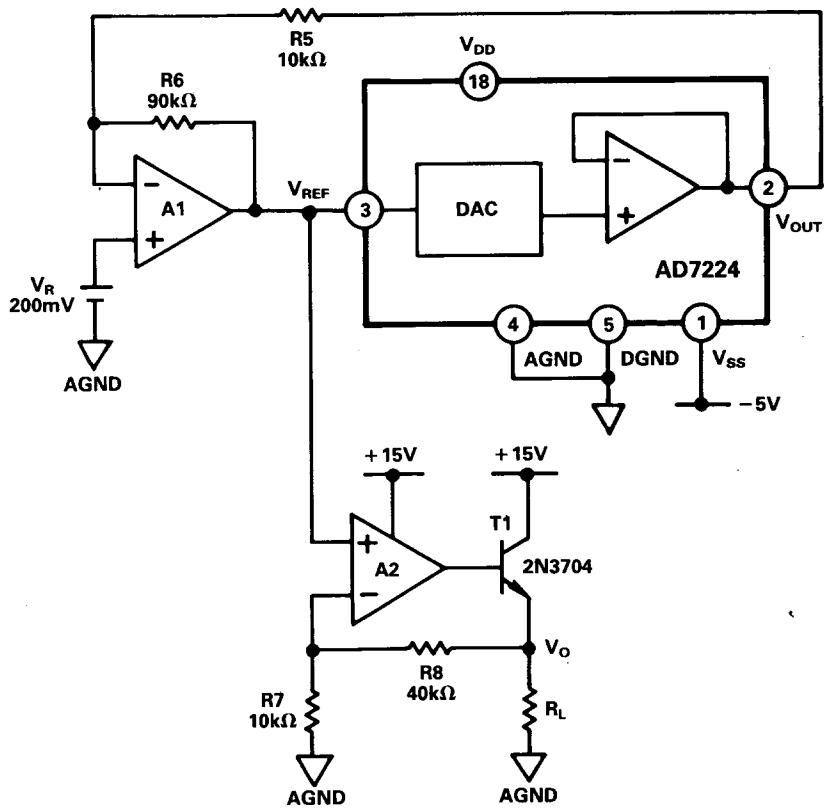

Figure 4. Current-Boost Configuration