# 5-channel BTL driver for CD players

## BA6795FP

The BA6795FP is a 5-channel BTL power driver for CD players and has an internal 5V regulator (attached PNP transistor required). The loading and spindle motor output pins are dual-use output pins and are switched between drivers using a control input. In addition, the internal level shifting circuit reduces the number of external components.

●Applications

CD players, CD-ROM drives and other optical disc devices

●Features

1) 5-channel BTL driver in a HSOP 28-pin package, ideal for application miniaturization.
2) Internal level shifting circuit reduces the number of external components.
3) Gain is adjustable with an attached resistor.
4) Internal thermal shutdown circuit.
5) Internal 5V regulator. (attached PNP transistor required)

●Absolute maximum ratings (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 18 | V |
| Power dissipation | Pd | 1.7*1 | W |
| Operating temperature | Topr | −35～+85 | ℃ |
| Storage temperature | Tstg | −55～+150 | ℃ |

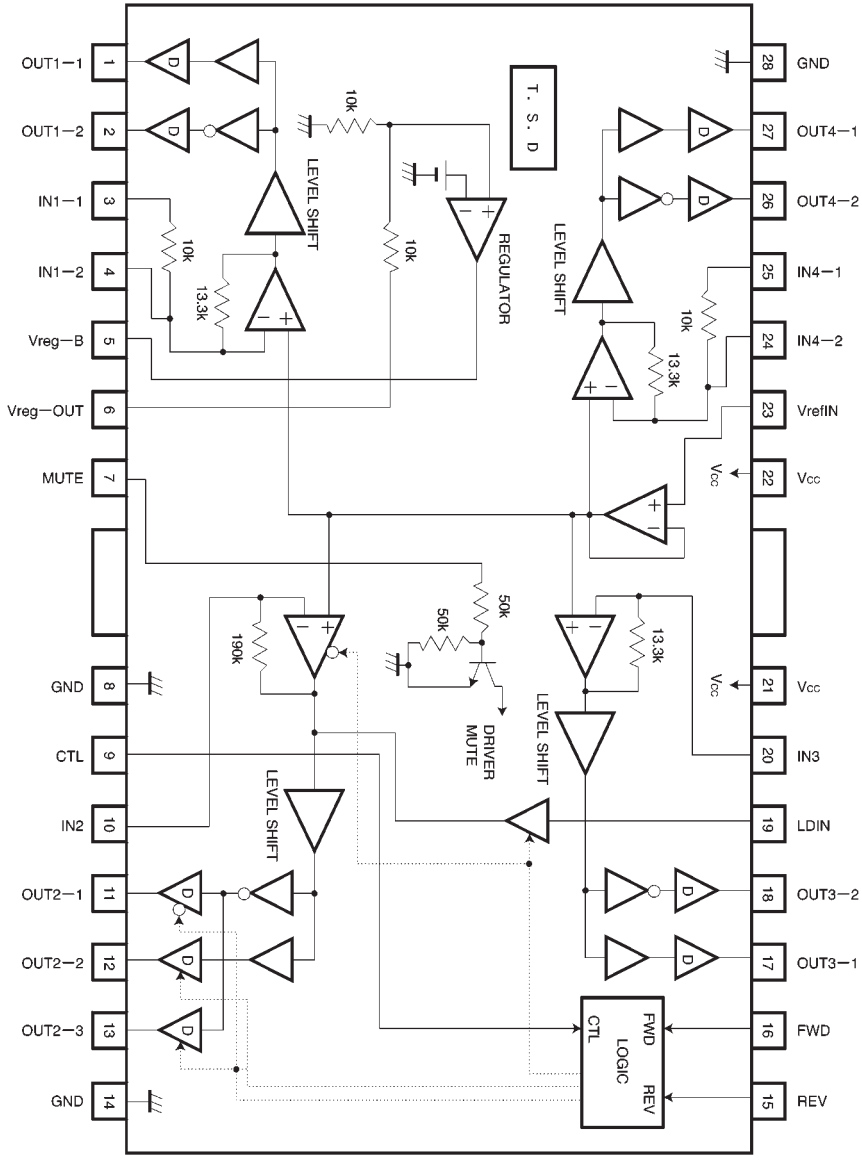
*1 When mounted on a 50 mm×50 mm×1.0 mm paper phenol board
Reduced by 13.6 mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 4.8 | — | 12.0 | V |
| | | 6.0 | — | 12.0 | V*2 |

*2 Without regulator

●Block diagram



●Pin descriptions

| Pin No. | Pin name | Function |
|---|---|---|
| 1 | OUT−1 | Channel 1 negative output |
| 2 | OUT−2 | Channel 1 positive output |
| 3 | IN 1−1 | Channel 1 input |
| 4 | IN 1−2 | Channel 1 gain adjustment input |
| 5 | Vreg−B | Attached transistor base connection |
| 6 | Vreg−OUT | Constant voltage output (attached transistor collector connection) |
| 7 | MUTE | Mute-on control |
| 8 | GND | Ground |
| 9 | CTL | Loading/spindle switching |
| 10 | IN 2 | Channel 2 gain adjustment input |
| 11 | OUT−1 | Channel 2 positive output |
| 12 | OUT−2 | Channel 2 negative output/Loading positive output |
| 13 | OUT−3 | Loading negative output |
| 14 | GND | Substrate ground |
| 15 | REV | Loading reverse input |
| 16 | FWD | Loading forward input |
| 17 | OUT3−1 | Channel 3 negative output |
| 18 | OUT3−2 | Channel 3 positive output |
| 19 | LDIN | Loading input |
| 20 | IN 3 | Channel 3 gain adjustment input |
| 21 | $V_{CC}$ | Vcc |
| 22 | $V_{CC}$ | Vcc |
| 23 | VrefIN | Bias amplifier input |
| 24 | IN 4−2 | Channel 4 gain adjustment input |
| 25 | IN 4−1 | Channel 4 input |
| 26 | OUT4−2 | Channel 4 positive output |
| 27 | OUT4−1 | Channel 4 negative output |
| 28 | GND | Substrate ground |

Note 1: Positive and negative output is relative to the polarity of the input pins.

Note 2: Loading positive output and loading negative output indicate the phase relative to the mode.

●Electrical characteristics (unless otherwise noted, Ta = 25°C, $V_{CC}$ = 8V, f = 1kHz, $R_L$ = 8Ω)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Quiescent current dissipation | $I_{CC}$ | 7.0 | 10.0 | 13.0 | mA | No load |
| Mute-off voltage | $V_{MOFF}$ | 2.0 | — | — | V | |
| Mute-on voltage | $V_{MON}$ | — | — | 0.5 | V | |
| 〈Drivers (other than loading drive)〉 | | | | | | |
| Output offset voltage 1 | $V_{OO1}$ | −40 | — | 40 | mV | Channels 1, 3 and 4, Driver |
| Output offset voltage 2 | $V_{OO2}$ | −60 | — | 60 | V | Channel 2 driver (spindle) |
| Maximum output voltage 1 | $V_{OH1}$ | 3.8 | 4.3 | — | V | $V_{IN}$=8V |
| Maximum output voltage 2 | $V_{OH2}$ | — | −4.3 | −3.8 | V | $V_{IN}$=0.7V |
| Closed loop voltage gain 1 | $G_{VC1}$ | 5.5 | 8.0 | 10.5 | dB | $V_{IN}$= μ0.5V *1 |
| Closed loop voltage gain 2 | $G_{VC2}$ | 7.5 | 11.0 | 14.5 | dB | $V_{IN}$= μ0.5V *2 |
| Ripple rejection | RR | — | 60 | — | dB | $V_{IN}$=0.1$V_{rms}$, 100Hz |
| Slew rate | SR | — | 2.0 | — | V/μs | 100 Hz square wave, 3$V_{P-P}$ output |
| 〈Loading drivers〉 | | | | | | |
| Output voltage F | $V_{OF}$ | 2.7 | 3.2 | 3.7 | V | $V_{CC}$=8V, RL=45Ω, VLD=3.0V |
| Output voltage R | $V_{OR}$ | −2.5 | −3.0 | −3.5 | V | |
| Output voltage range F | $V_{OMF}$ | 1.9 | 2.2 | — | V | $V_{CC}$=8V, RL=45Ω, VLD=4.5V*3 |
| Output voltage range R | $V_{OMR}$ | — | −2.2 | −1.9 | V | |
| Output load variation F1 | $\Delta V_{F1}$ | — | 250 | 500 | mV | $V_{CC}$=8V, VLD=3.0V I=100→400mA*4 |
| Output load variation R1 | $\Delta V_{R1}$ | — | 250 | 500 | mV | |
| Output load variation F2 | $\Delta V_{F2}$ | — | 600 | 850 | mV | $V_{CC}$=5V, VLD=4.5V I=100→400mA*5 |
| Output load variation R2 | $\Delta V_{R2}$ | — | 600 | 850 | mV | |
| Supply voltage variation F | $\Delta V_{FL}$ | −500 | — | 500 | mV | $V_{CC}$=4.8V→12V, RL=∞ |
| Supply voltage variation R | $\Delta V_{RL}$ | −500 | — | 500 | mV | |
| Output offset voltage | $V_{OOL}$ | −50 | 2.0 | 50 | mV | When braking: Output voltage |
| 〈Controllers CTL, FWD and REV〉 | | | | | | |
| Input high level voltage 1 | $V_{IH1}$ | 2.0 | — | — | V | FWD (pin 16), REV (pin 15) Determined by input pin voltage |
| Input low level voltage 1 | $V_{IL1}$ | — | — | 0.5 | V | |
| Input high level voltage 2 | $V_{IH2}$ | 4.0 | — | — | V | CTL (pin 9) Determined by input pin voltage |
| Input low level voltage 2 | $V_{IL2}$ | — | — | 0.5 | V | |
| Input high level current | $I_{IH}$ | — | — | 500 | μA | $V_{IN}$=5V |
| Input low levelcurrent | $I_{IL}$ | — | — | 500 | μA | $V_{IN}$=0V |
| 〈5 V regulator〉 | | | | | | |
| Output voltage | Vreg | 4.75 | 5.00 | 5.25 | V | $I_L$=100mA |
| Output load variation | $\Delta V_{RL}$ | −50 | 0 | 50 | mV | $I_L$=0～200mA |
| Supply voltage variation | $\Delta V_{VCC}$ | −50 | 0 | 25 | mV | ($V_{CC}$=6～9V) $I_L$=100mA |

◎Not designed for radiation resistance.

*1 Attach a 10 kΩ resistor to the inputs (channel 1, channel 3 and channel 4).

*2 Attach a 100 kΩ resistor to the inputs (channel 2).

*3 $V_{omf}$ and $V_{omr}$ remain roughly the same even when loading input VLD (pin 19) is opened.

*4 $\Delta V_{f1}$, $\Delta V_{r1}$ indicate load variation at unclipped, 3.0 V output.

*5 $\Delta V_{f2}$, $\Delta V_{r2}$ indicate load variation when output is clipped to generate 4.5 V input at reduced voltage (5 V).

●Measruement circuit

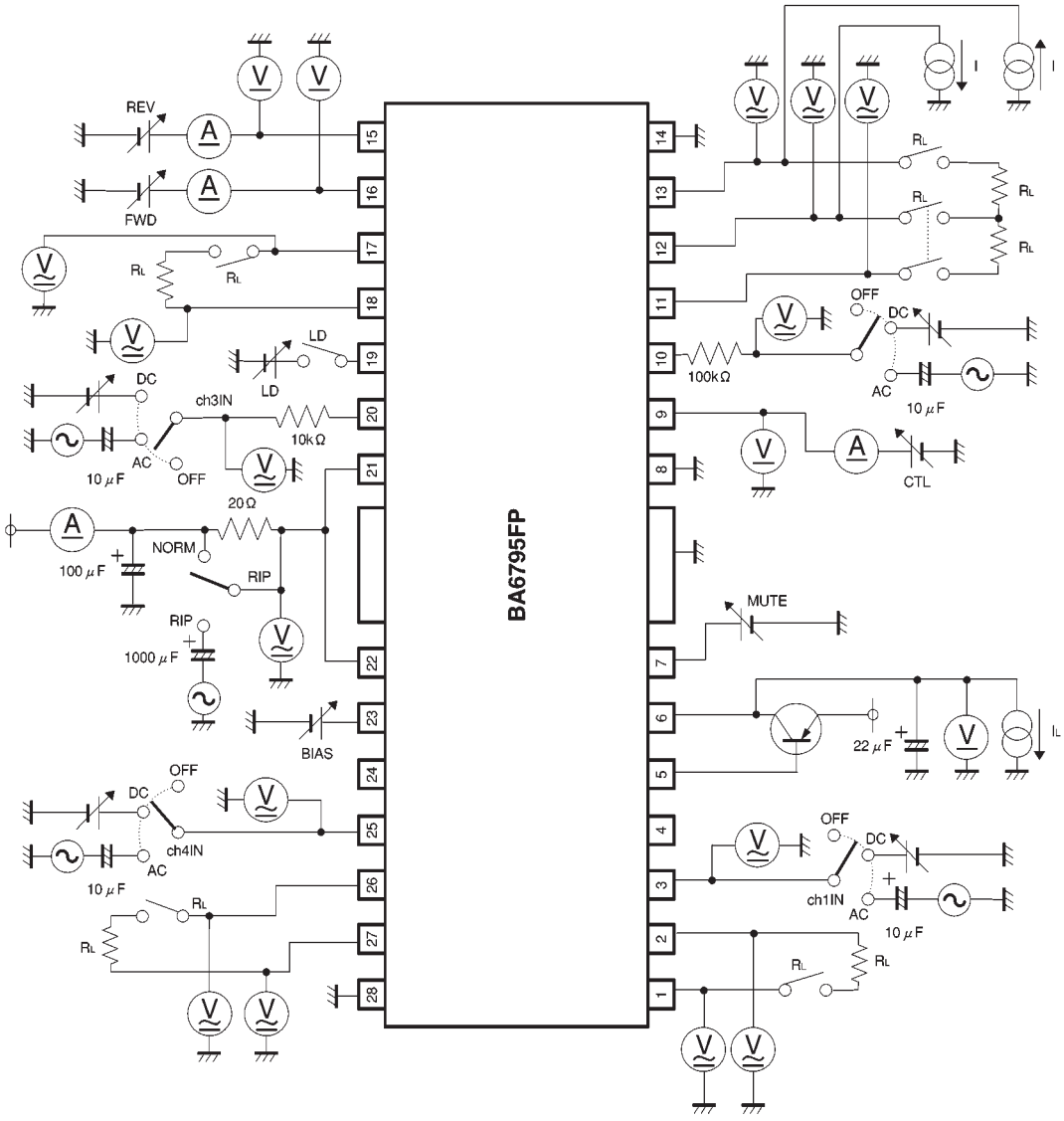



Fig.1

●Measruement circuit switch table

| Parameter | Switch | | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | RL | RL' | LD | RIP | CH1 | CH2 | CH3 | CH4 | |
| Quiescent current dissipation | OFF | OFF | OFF | NORM | OFF | OFF | OFF | OFF | |
| Mute-off voltage | ON | ON | ↓ | ↓ | DC | DC | DC | DC | DC : Vcc or GND |
| Mute-on voltage | ON | ON | ↓ | ↓ | DC | DC | DC | DC | DC : Vcc or GND |
| 〈Drivers (other than loading driver)〉 | | | | | | | | | |
| Output offset voltage | ON | ON | OFF | NORM | DC | DC | DC | DC | DC: bias voltage |
| Maximum output voltage | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC : Vcc or 0.7V |
| Closed loop voltage gain 1 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias ±0.5 V |
| Closed loop voltage gain 2 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias ±0.5 V |
| Ripple rejection | ↓ | ↓ | ↓ | RIP | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Slew rate | ↓ | ↓ | ↓ | NORM | AC | AC | AC | AC | AC: 100 Hz square wave |
| 〈Loading drivers〉 | | | | | | | | | |
| Output voltage F | ON | ON | ON | NORM | OFF | DC | OFF | OFF | DC: bias voltage |
| Output voltage R | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Output voltage range F | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Output voltage range R | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Load regulation F | ↓ | OFF | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Load regulation R | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Line regulation | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage |
| Output offset voltage | ↓ | ON | OFF | ↓ | ↓ | ↓ | ↓ | ↓ | DC: bias voltage (brake mode) |
| 〈Controller pins〉 | | | | | | | | | |
| Input high level voltage 1 | ON | ON | OFF | NORM | OFF | DC | OFF | OFF | |
| Input low level voltage 1 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | |
| Input high level voltage 2 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | |
| Input low level voltage 2 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | |
| Input low level current | OFF | OFF | OFF | ↓ | ↓ | OFF | ↓ | ↓ | |
| 〈5 V regulator〉 | | | | | | | | | |
| Output voltage | OFF | OFF | OFF | NORM | OFF | OFF | OFF | OFF | |
| Load regulation | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | |
| Line regulation | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | |

∗ When measuring drivers (excluding loading driver), CTL voltage should be under 0.5 V.

∗ I and $I_L$, used in the test circuit diagram, are the same as the symbols used in electrical characteristics table.

●Circuit operation

(1) Switching between spindle and loading motor driver output modes ($V_{CC}$ = 8V)

| CTL | FWD | REV | Spindle | Loading | | Dimentions |
|---|---|---|---|---|---|---|
| L | L | L | ON | OFF | | Fig. 2 |
| | | H | | | | |
| | H | L | | | | |
| | | H | | | | |
| H | L | L | OFF | OFF | High impedance | Fig. 3 |
| | | H | | ON | Reverse | Fig. 4 |
| | H | L | | | Forward | Fig. 5 |
| | | H | | | Brake | Fig. 6 |

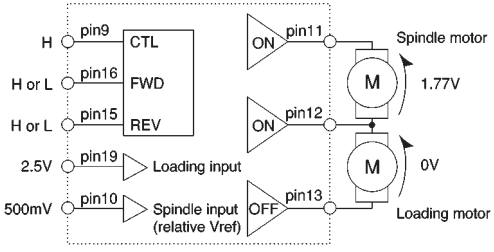



Fig. 2

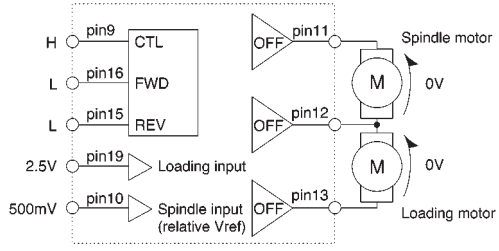



Fig.3

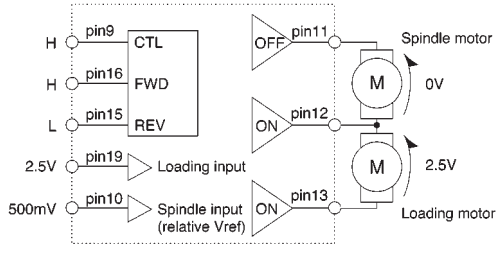



Fig. 4

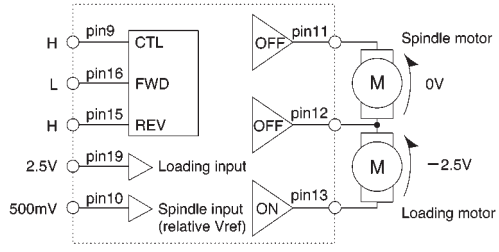



Fig. 5

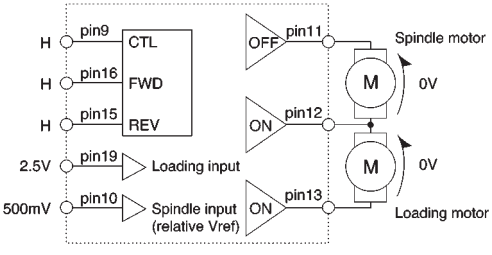
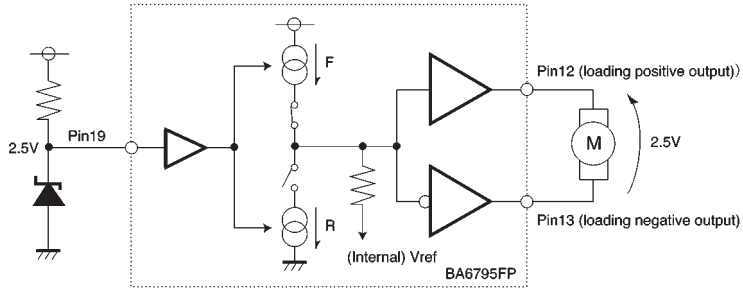



Fig. 6

Note: Gains for spindle driver (channel 2) and loading driver are 11dB and 0dB, respectively.

●Circuit operation

(2) Loading motor driver voltage setting (forward mode)




Input voltage = output voltage (gain: 0 dB)

Note: When the loading input pin (pin 19) is opened, a voltage corresponding to the dynamic range of the power supply being used is output according to the mode.

Fig. 7

●Application example

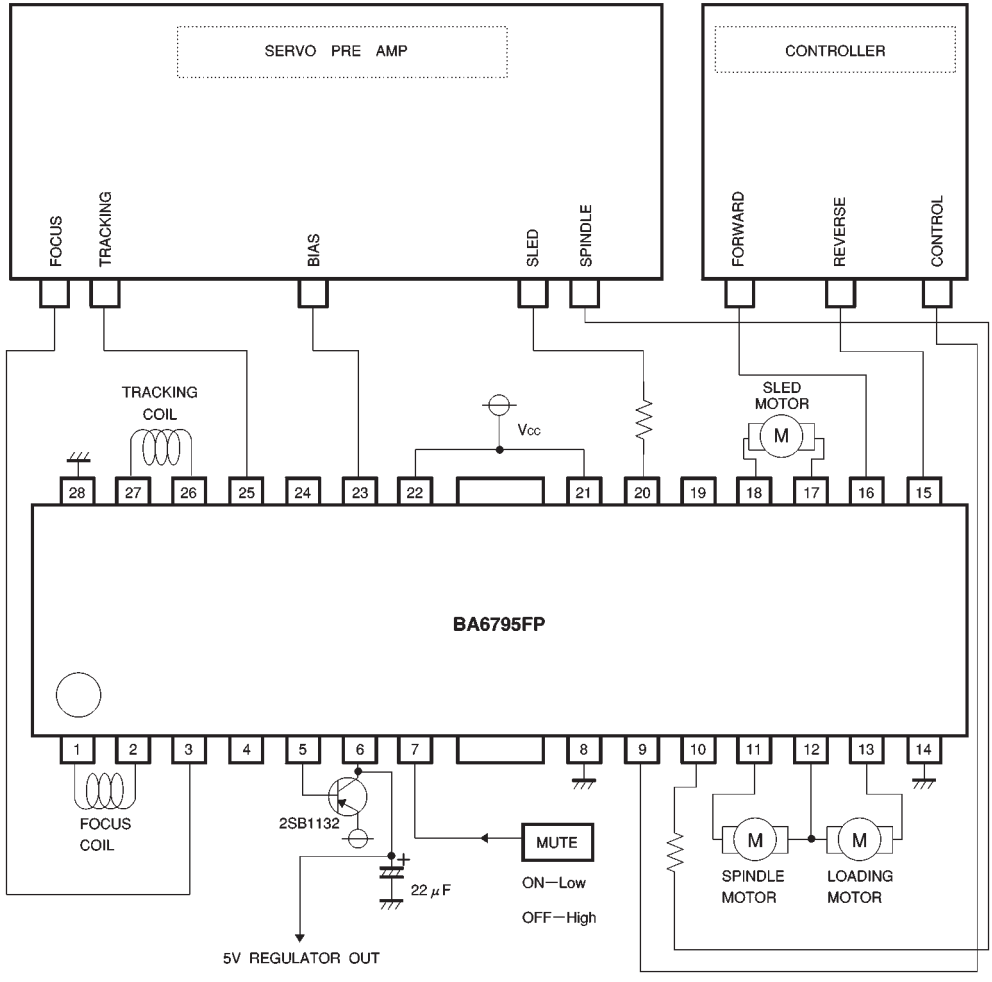



Fig.8

●Operation notes

(1) The BA6795FP has an internal thermal shutdown circuit. Output current is muted when the chip temperature exceeds 175°C (typically).

(2) If the mute pin (pin 7) voltage is opened or lowered below 0.5V, the output current will be muted. Pin 7 should be pulled up above 2.0V during normal use.

(3) The bias pin (pin 23) is muted when lowered below 1.4V (typically). Make sure it stays above 1.6V during normal use.

(4) Muting occurs during thermal shutdown, mute-on operations or a drop in the bias pin voltage or supply voltage. In each case, only the drivers are muted. During muting, the output pins remain at the internal bias voltage, roughly $(V_{CC}–V_F)/2$.

(5) The driver circuit shuts down when the supply voltage drops below 4.3V (typically), and starts up again when the voltage rises above 4.5V (typically).

(6) Fluctuation due to temperature occurs in the gain when using an attached resistor as the input resistor for a driver other than the spindle driver (typically 2200ppm per degree) or for the spindle driver (typically 4600ppm per degree. (Only when using the gain adjustment pin.)

(7) Be sure to connect the IC to a 0.1μF bypass capacitor to the power supply, at the base of the IC.

(8) The radiating fin is connected to the package's internal GND, but should also be connected to an external ground.

(9) The capacitor between regulator output (pin 6) and GND also serves to prevent oscillation of the IC, so select one with good temperature characteristics.

●Electrical characteristic curves

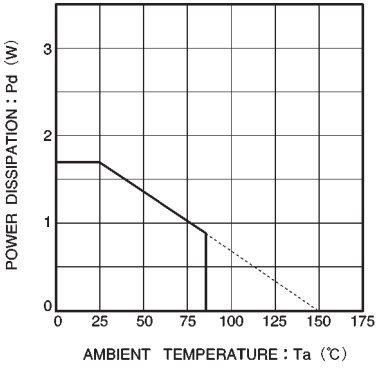



Fig. 9 Thermal derating curve

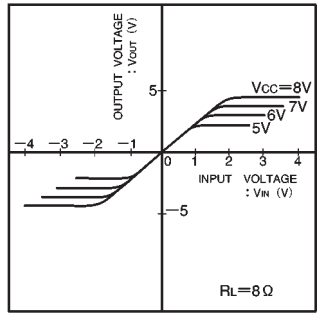



Fig. 10 Driver I / O characteristics (when load changes) (except channel 2)

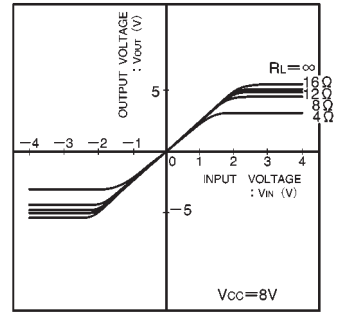



Fig. 11 Driver I / O characteristics (when power supply voltage power changes) (except channel 2)

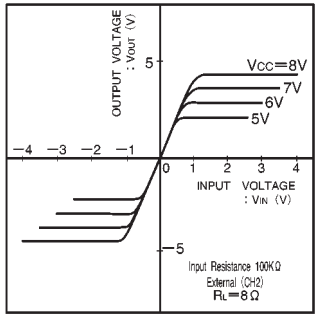



Fig. 12 Driver I / O characteristics (channel 2)

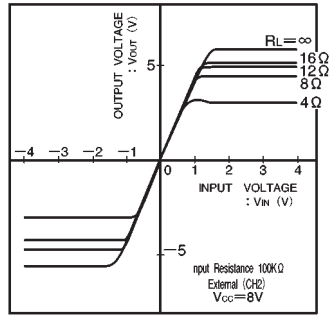
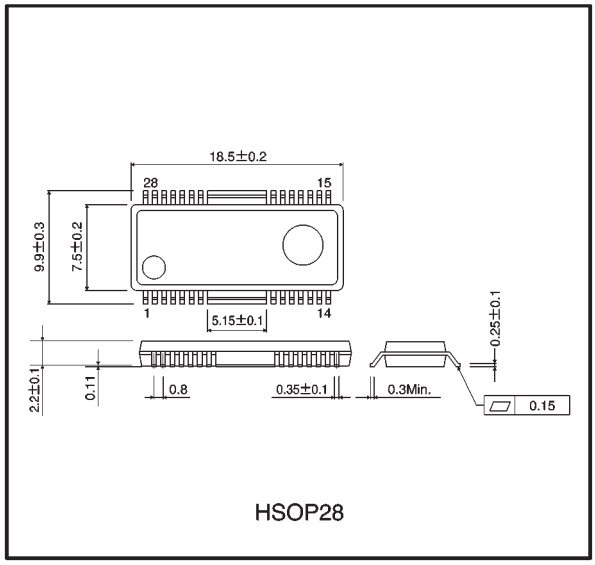



Fig. 13 Driver I / O characteristics (channel 2)

●External dimensions (Units: mm)




HSOP28