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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HAT3010R

Silicon N/P Channel Power MOS FET
High Speed Power Switching

RENESAS

ADE-208-1402H (Z)

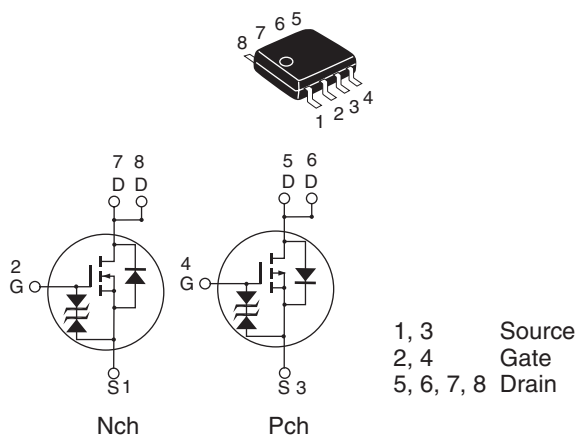
9th. Edition
Aug. 2002

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V _{DSS}	60	-60	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	6	-5	A
Drain peak current	I _{D(pulse)} ^{Note1}	48	-40	A
Body-drain diode reverse drain current	I _{DR}	6	-5	A
Channel dissipation	Pch ^{Note2}	2	2	W
Channel dissipation	Pch ^{Note3}	3	3	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	-55 to +150	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1 %

2. 1 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

3. 2 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

Electrical Characteristics (Ta = 25°C)

• N Channel

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	25	32	$\text{m}\Omega$	$I_D = 3 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	32	45	$\text{m}\Omega$	$I_D = 3 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	7	11	—	S	$I_D = 3 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	Ciss	—	1050	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	150	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	90	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$
Rise time	t_r	—	15	—	ns	$V_{DD} \approx 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	$R_L = 10 \Omega$
Fall time	t_f	—	10	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.10	V	$I_F = 6 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 6 \text{ A}, V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

HAT3010R

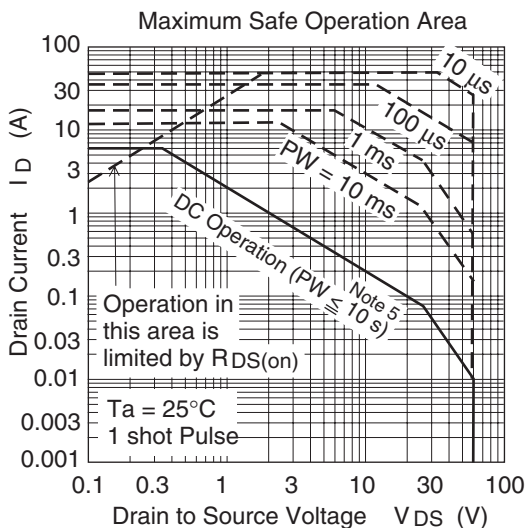
• P Channel

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -60 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	60	76	$\text{m}\Omega$	$I_D = -2.5 \text{ A}, V_{GS} = -10 \text{ V}$ ^{Note5}
	$R_{DS(on)}$	—	90	130	$\text{m}\Omega$	$I_D = -2.5 \text{ A}, V_{GS} = -4.5 \text{ V}$ ^{Note5}
Forward transfer admittance	$ y_{fs} $	3	5	—	S	$I_D = -2.5 \text{ A}, V_{DS} = -10 \text{ V}$ ^{Note5}
Input capacitance	C_{iss}	—	1350	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	135	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	85	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = -10 \text{ V}, I_D = -2.5 \text{ A}$
Rise time	t_r	—	15	—	ns	$V_{DD} \approx -30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	$R_L = 12 \text{ }\Omega$
Fall time	t_f	—	10	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	-0.85	-1.10	V	$I_F = -5 \text{ A}, V_{GS} = 0$ ^{Note5}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = -5 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

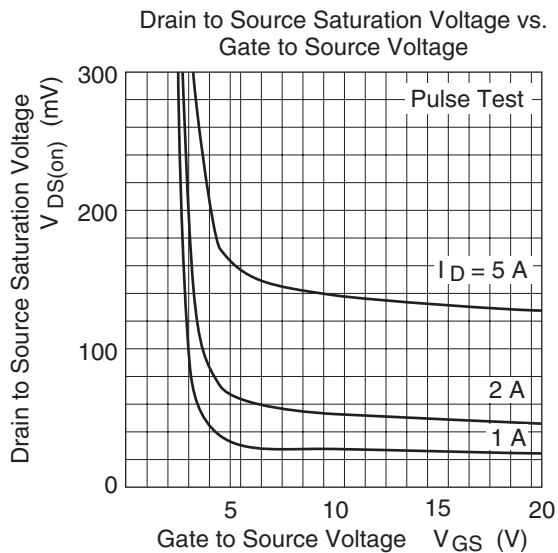
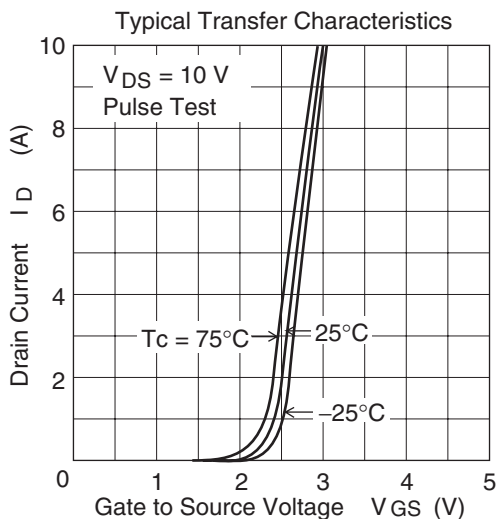
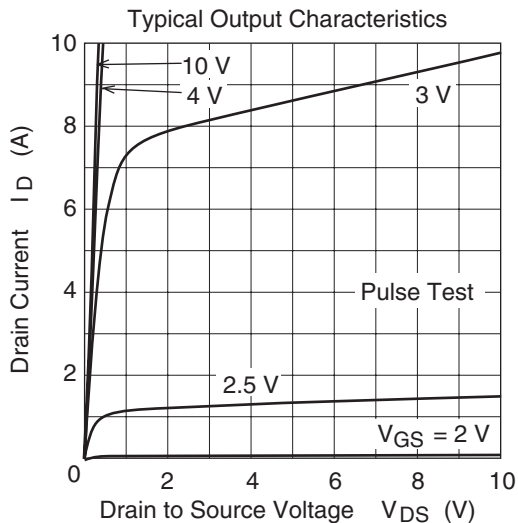
Notes: 5. Pulse test

Main Characteristic

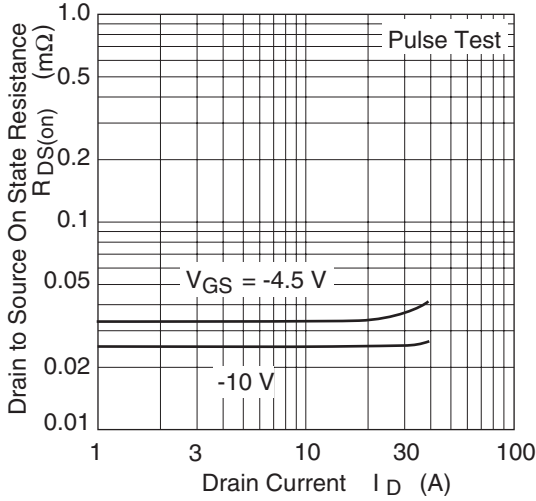
• N Channel



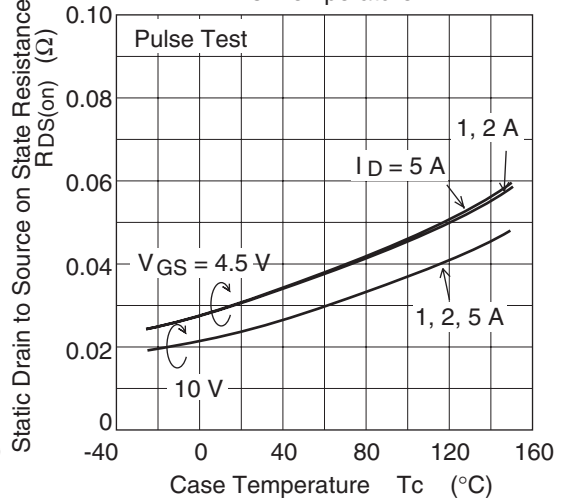
Note 5 :
When using the glass epoxy board (FR4 40 x 40 x 1.6 mm)



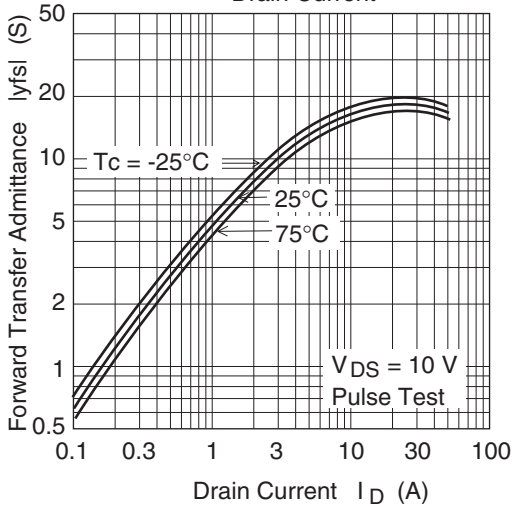
Static Drain to Source on State Resistance vs. Drain Current



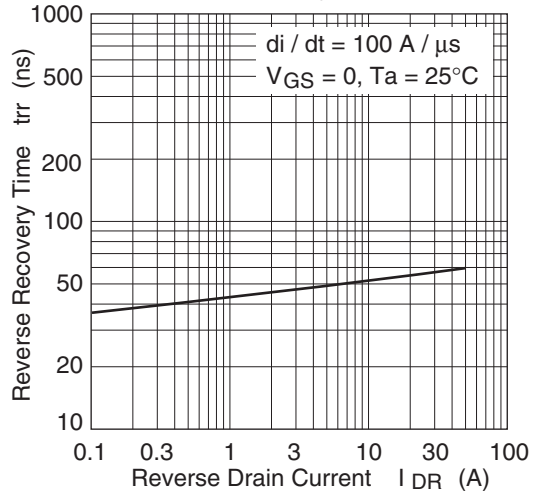
Static Drain to Source on State Resistance vs. Temperature



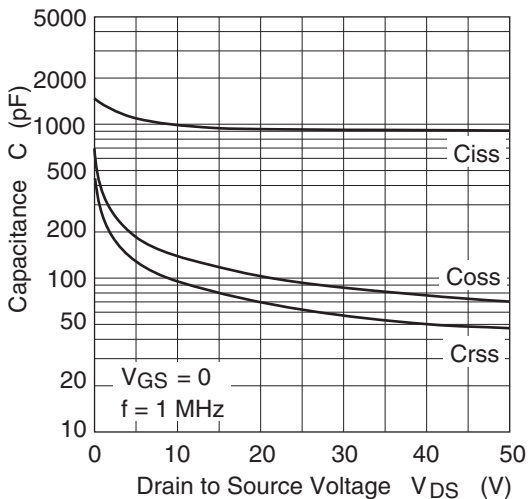
Forward Transfer Admittance vs. Drain Current



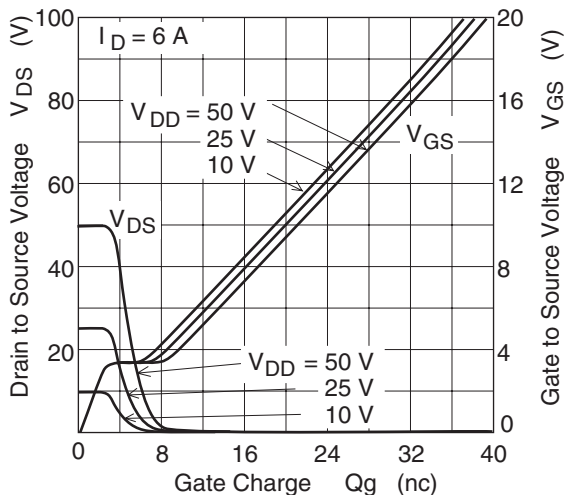
Body-Drain Diode Reverse Recovery Time



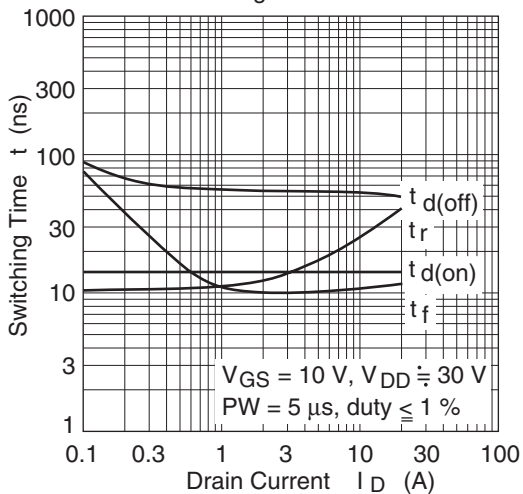
Typical Capacitance vs. Drain to Source Voltage



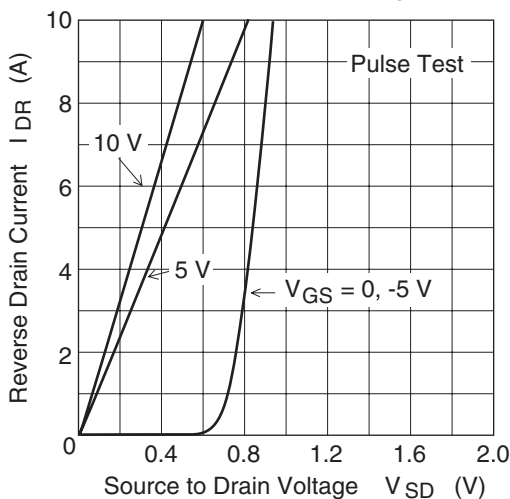
Dynamic Input Characteristics



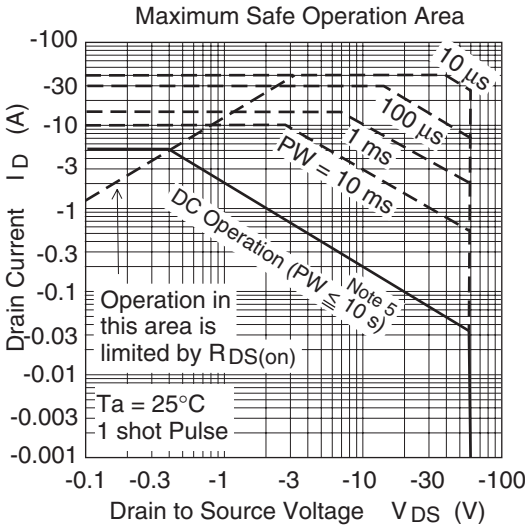
Switching Characteristics



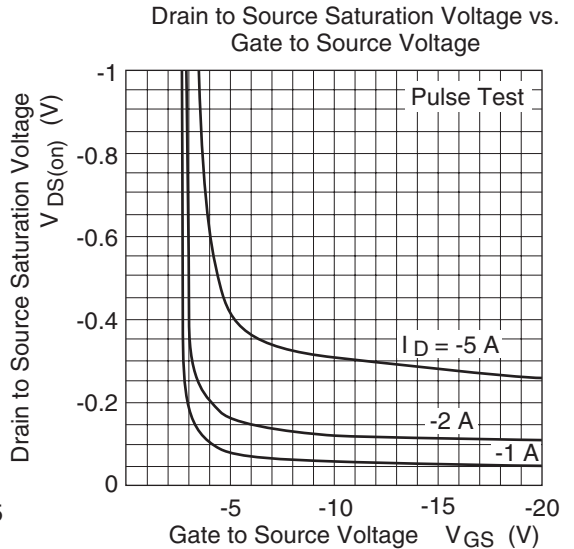
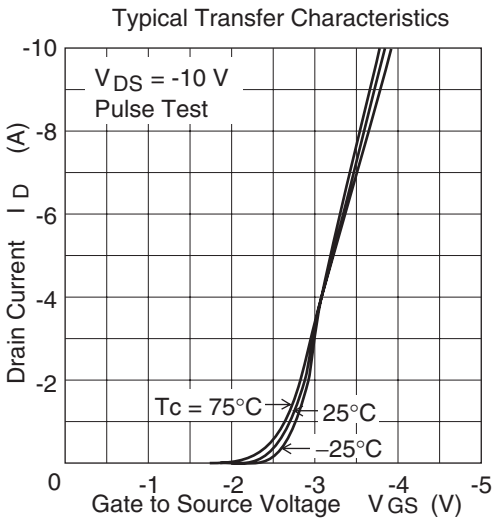
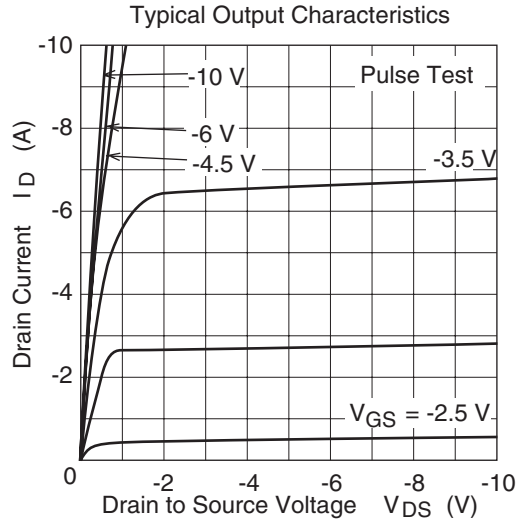
Reverse Drain Current vs. Source to Drain Voltage



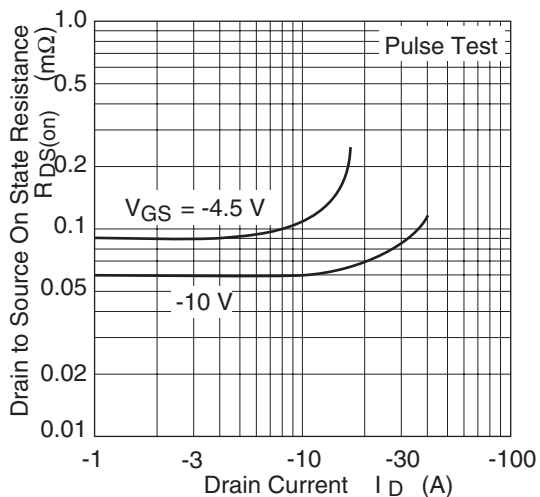
• P Channel



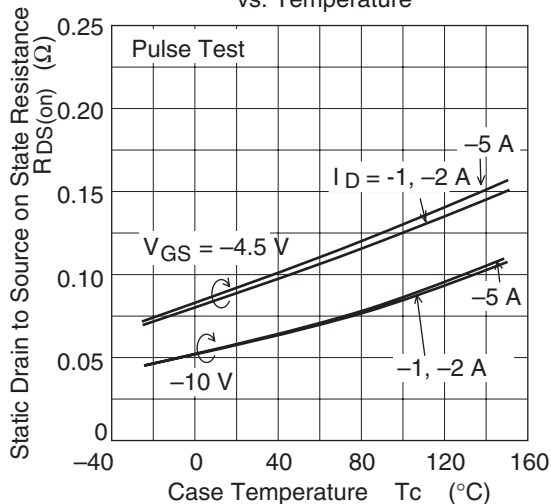
Note 5 :
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)



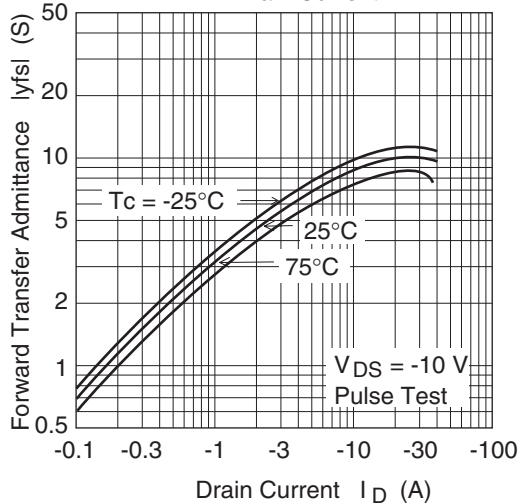
Static Drain to Source on State Resistance vs. Drain Current



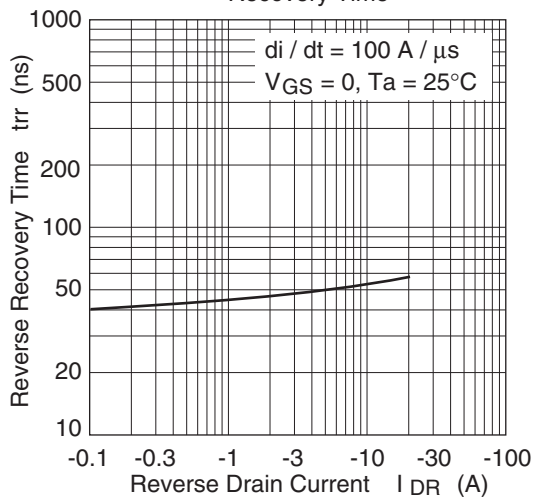
Static Drain to Source on State Resistance vs. Temperature



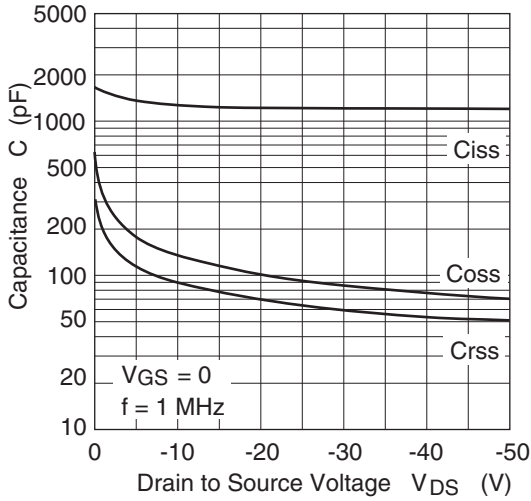
Forward Transfer Admittance vs. Drain Current



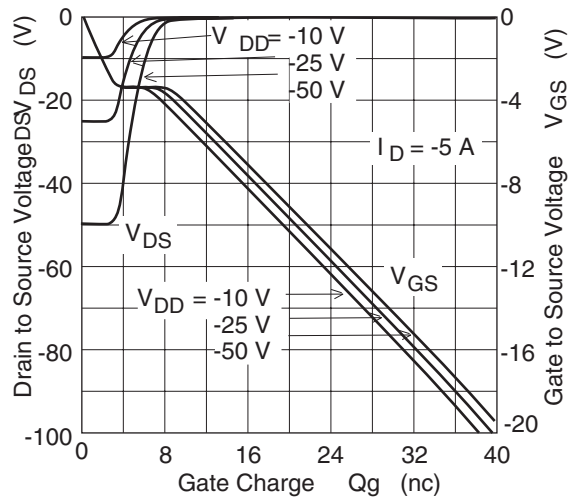
Body-Drain Diode Reverse Recovery Time



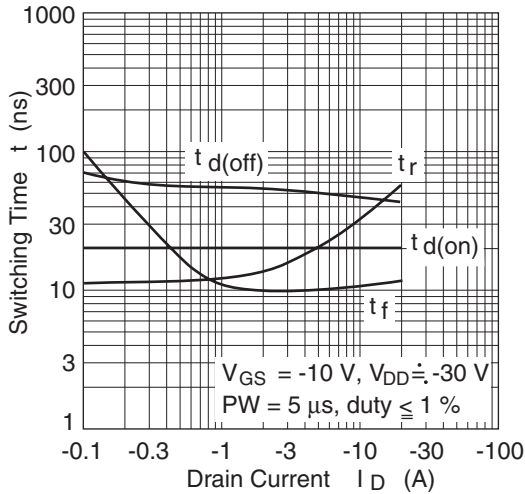
Typical Capacitance vs. Drain to Source Voltage



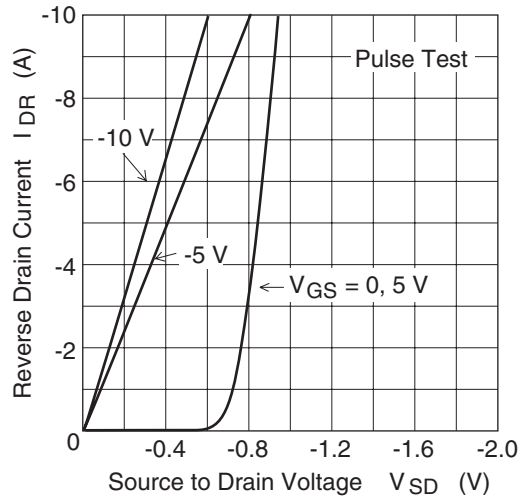
Dynamic Input Characteristics

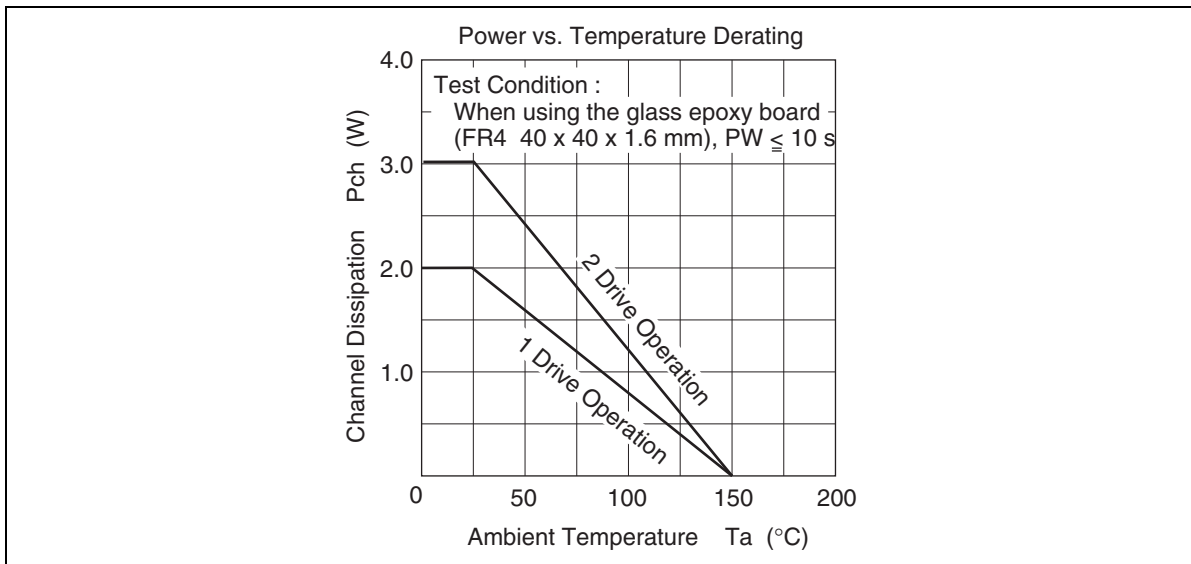


Switching Characteristics

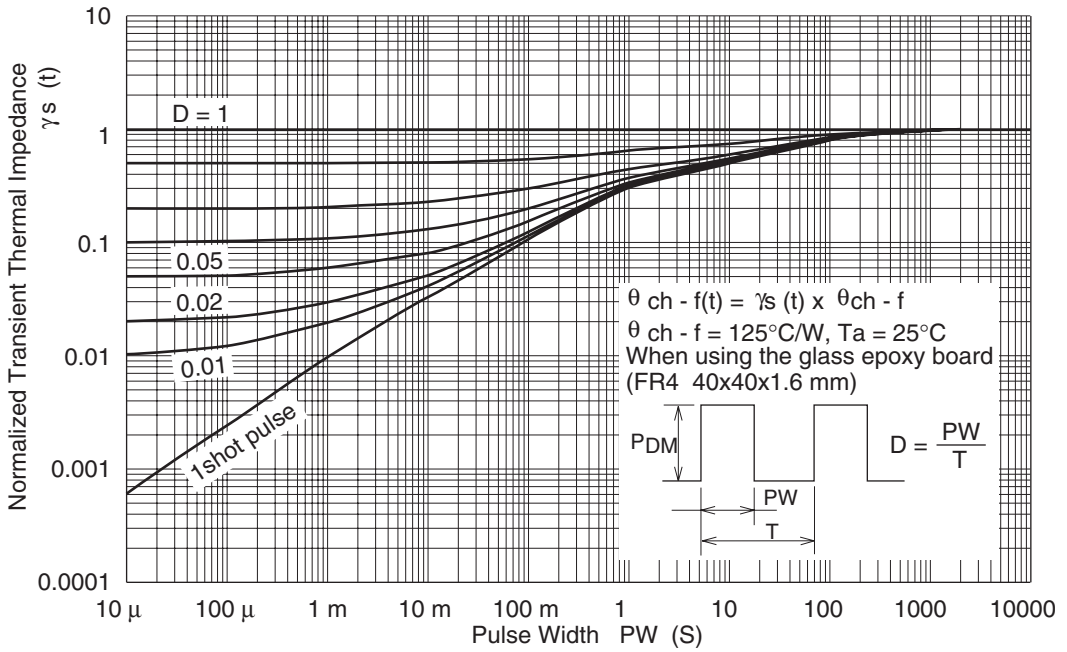


Reverse Drain Current vs. Source to Drain Voltage

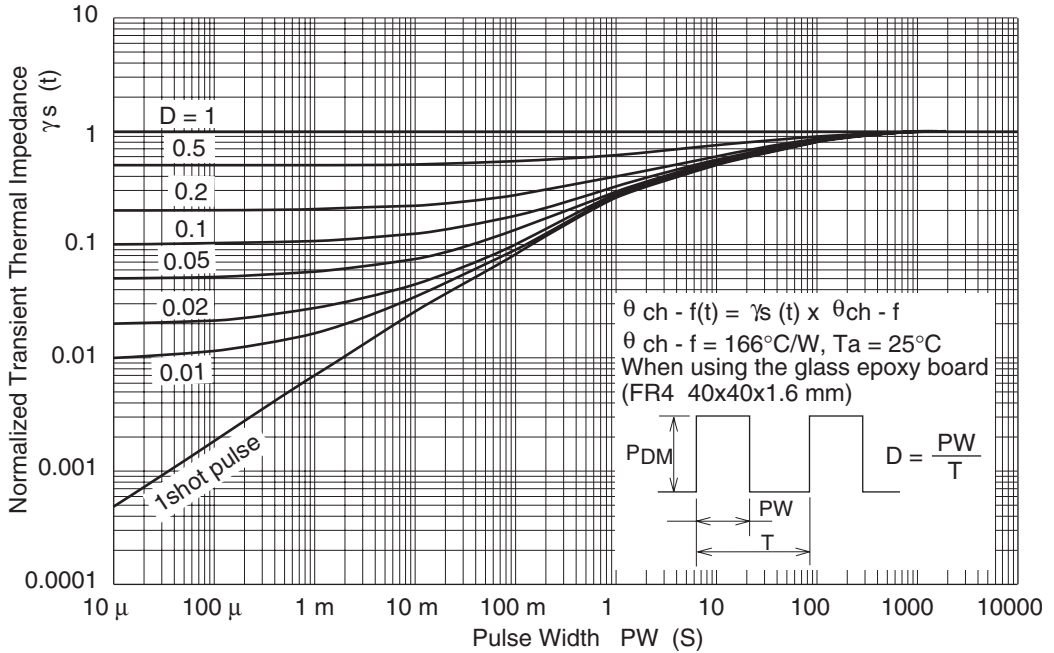




Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

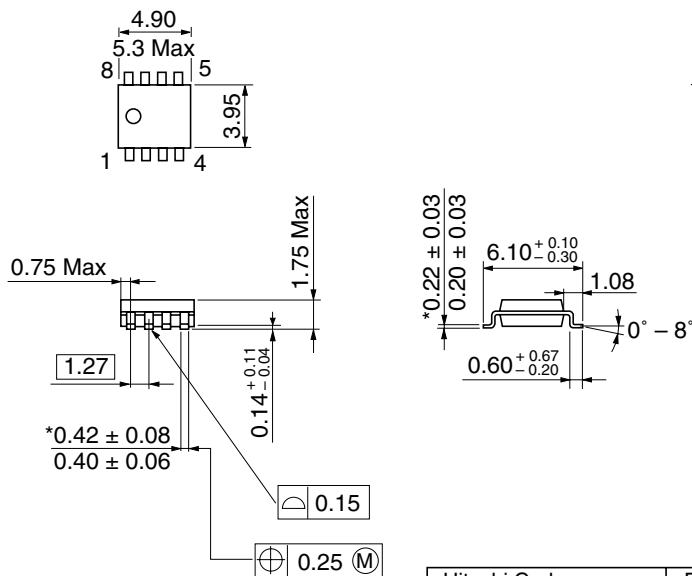


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions

As of January, 2002
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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