



IRF630M IRF630MFP

N-CHANNEL 200V - 0.35Ω - 9A TO-220/TO-220FP
MESH OVERLAY™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
IRF630M	200 V	< 0.40 Ω	9 A
IRF630FPM	200 V	< 0.40 Ω	9 A

- TYPICAL R_{DS(on)} = 0.35 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

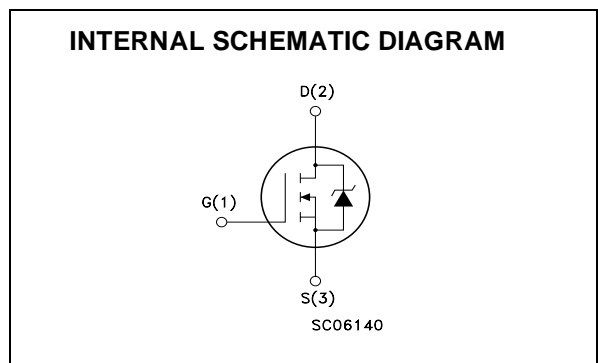
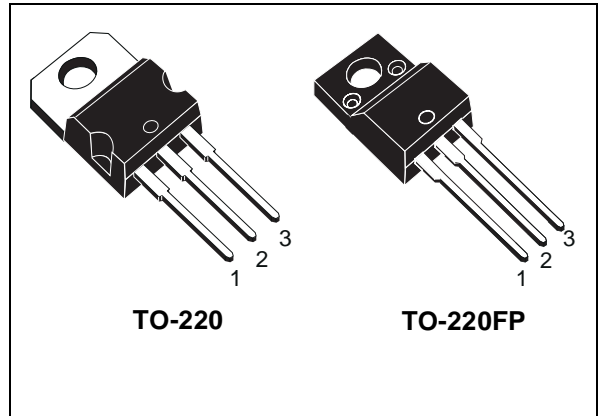
DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

Isolated TO-220 option simplifies assembly and cuts risk of accidental short circuit in crowded monitor PCB's.

APPLICATIONS

- MONITOR DISPLAYS
- GENERAL PURPOSE SWITCH



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		IRF630M	IRF630MFP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	200		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	200		V
V _{GS}	Gate- source Voltage	± 20		V
I _D	Drain Current (continuous) at T _C = 25°C	9	9 (**)	A
I _D	Drain Current (continuous) at T _C = 100°C	5.7	5.7 (**)	A
I _{DM} (●)	Drain Current (pulsed)	36	36	A
P _{TOT}	Total Dissipation at T _C = 25°C	75	30	W
	Derating Factor	0.6	0.24	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5	5	V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	--	2500	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 9A, di/dt ≤ 300A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(**) Limited only by Maximum Temperature Allowed

IRF630M / FP

THERMAL DATA

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1.67	4.17	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300		°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	200			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 4.5 A		0.35	0.40	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 4.5 A	3	4		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		540	700	pF
C _{oss}	Output Capacitance			90	120	pF
C _{rss}	Reverse Transfer Capacitance			35	50	pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 100\text{ V}, I_D = 4.5\text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		10	14	ns
t_r	Rise Time			15	20	ns
Q_g	Total Gate Charge	$V_{DD} = 160\text{ V}, I_D = 9\text{ A},$ $V_{GS} = 10\text{ V}$		31	45	nC
Q_{gs}	Gate-Source Charge			7.5		nC
Q_{gd}	Gate-Drain Charge			9		nC

SWITCHING OFF

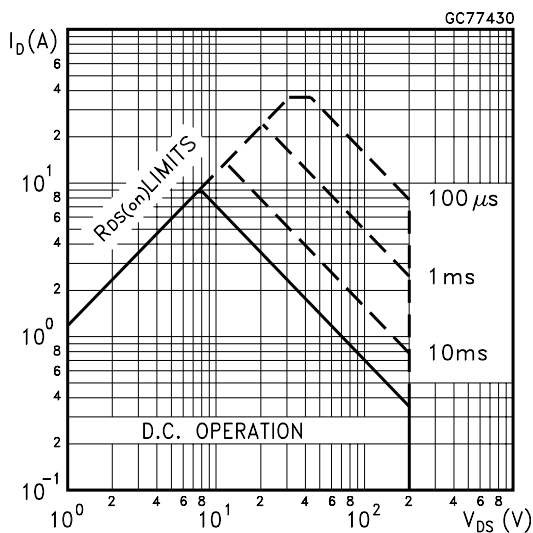
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 160\text{ V}, I_D = 9\text{ A},$ $R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		12	17	ns
t_f	Fall Time			12	17	ns
t_c	Cross-over Time			25	35	ns

SOURCE DRAIN DIODE

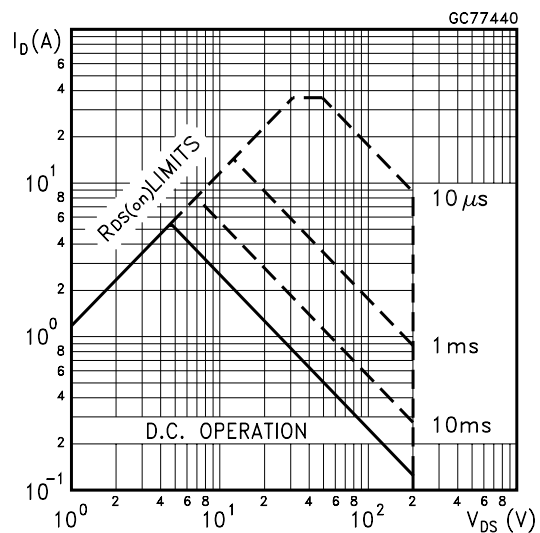
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				9	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				36	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 9\text{ A}, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}, T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		170		ns
Q_{rr}	Reverse Recovery Charge			0.95		μC
I_{RRM}	Reverse Recovery Current			11		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

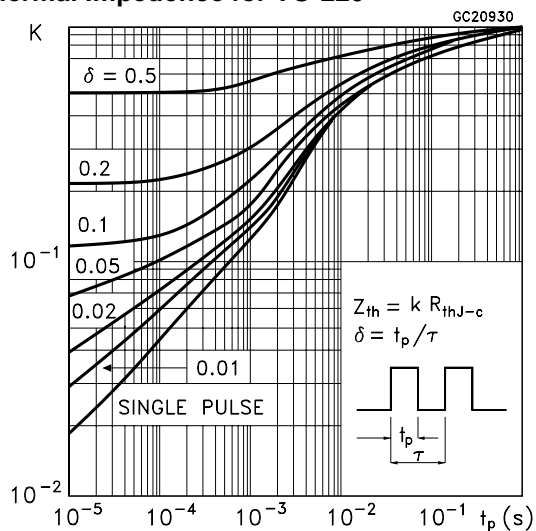
Safe Operating Area for TO-220



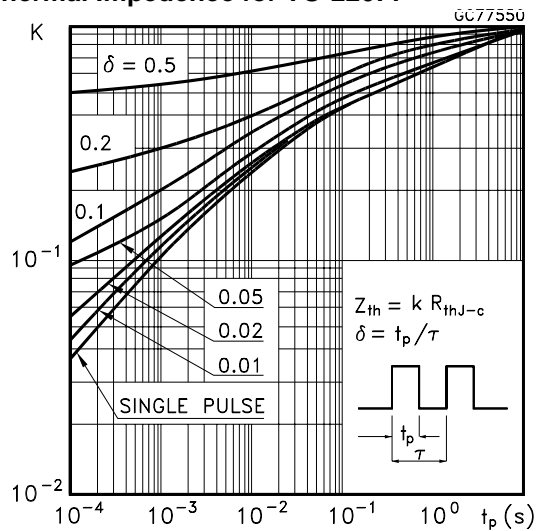
Safe Operating Area for TO-220FP



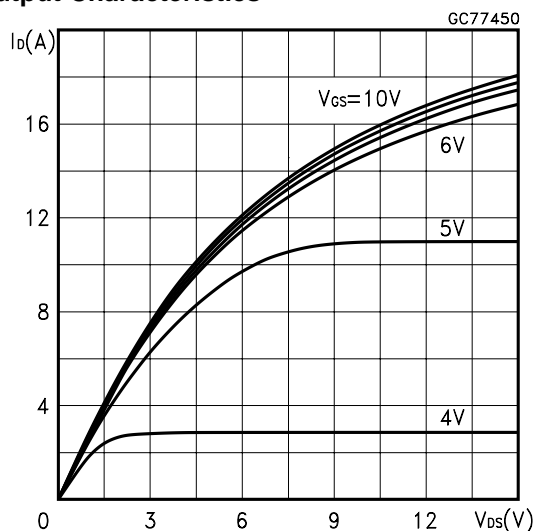
Thermal Impedance for TO-220



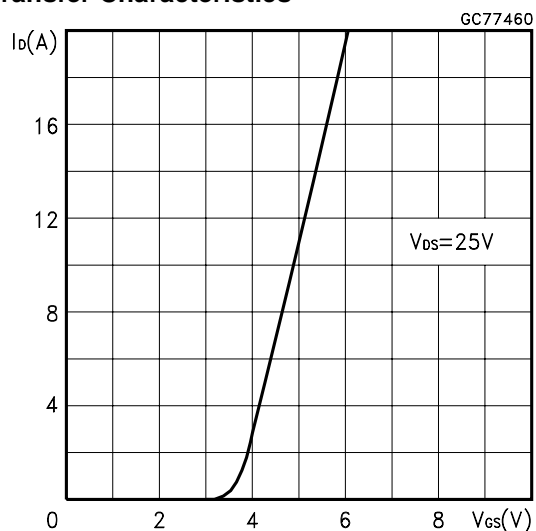
Thermal Impedance for TO-220FP



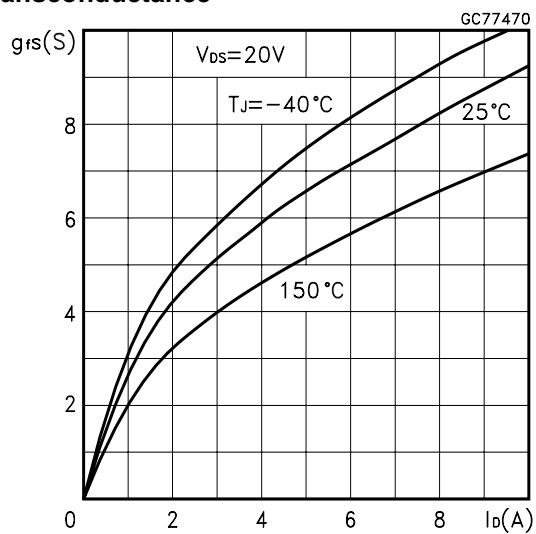
Output Characteristics



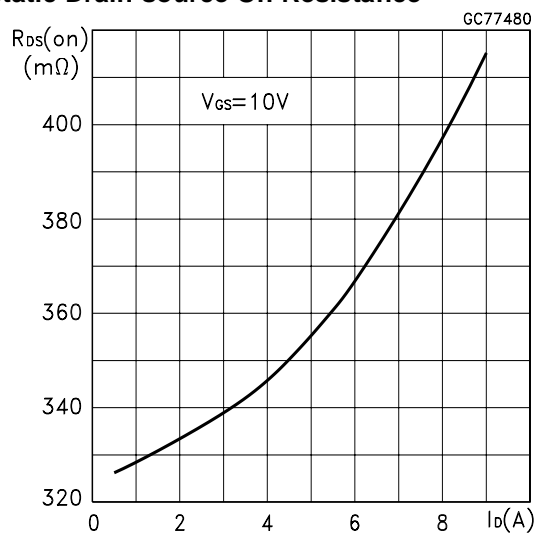
Transfer Characteristics



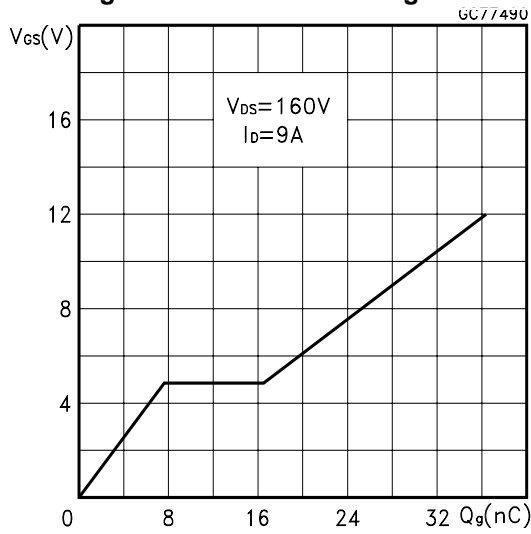
Transconductance



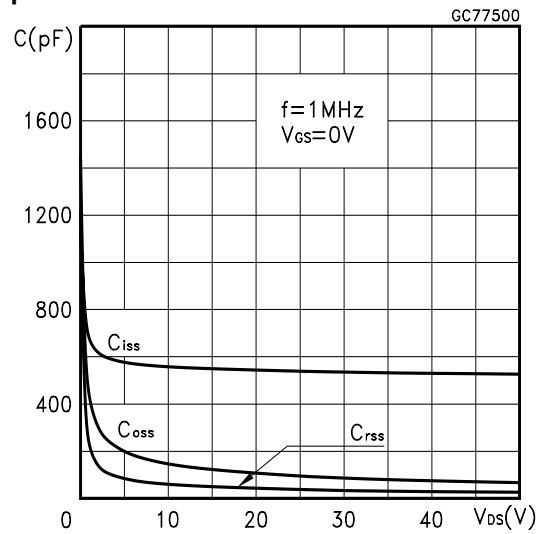
Static Drain-source On Resistance



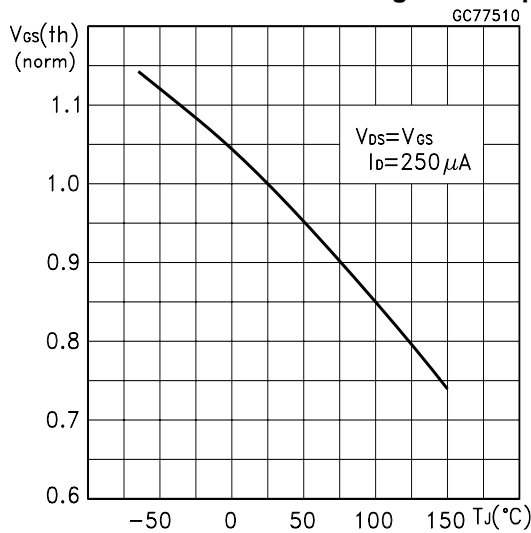
Gate Charge vs Gate-source Voltage



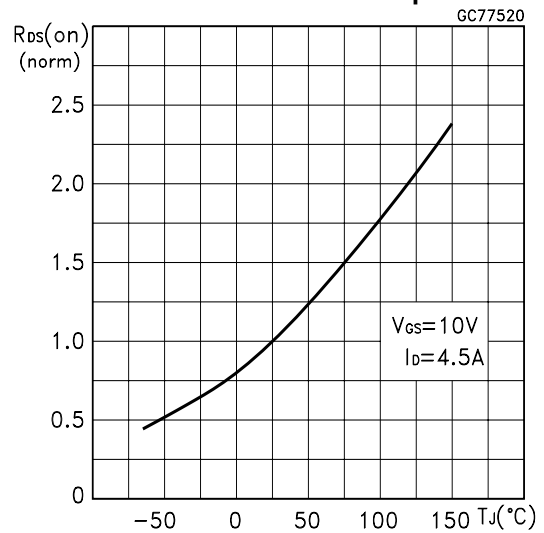
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

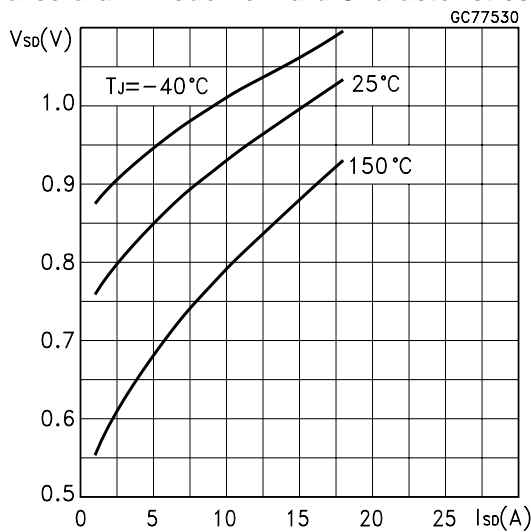


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load



Fig. 4: Gate Charge test Circuit

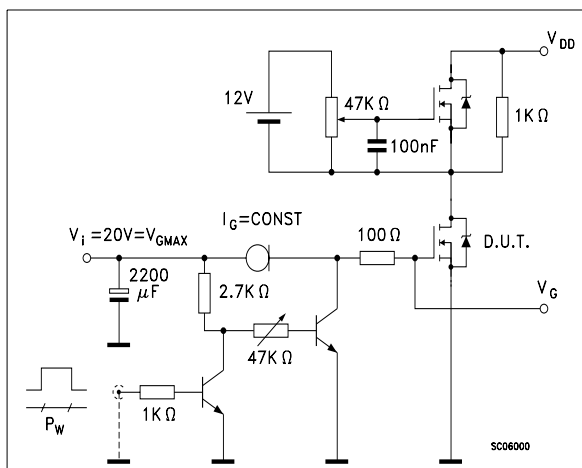
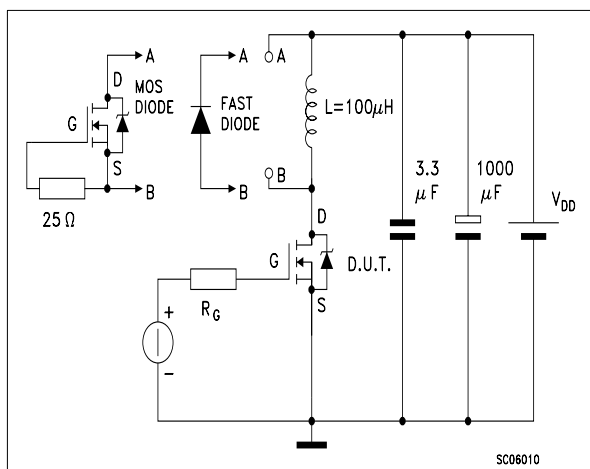
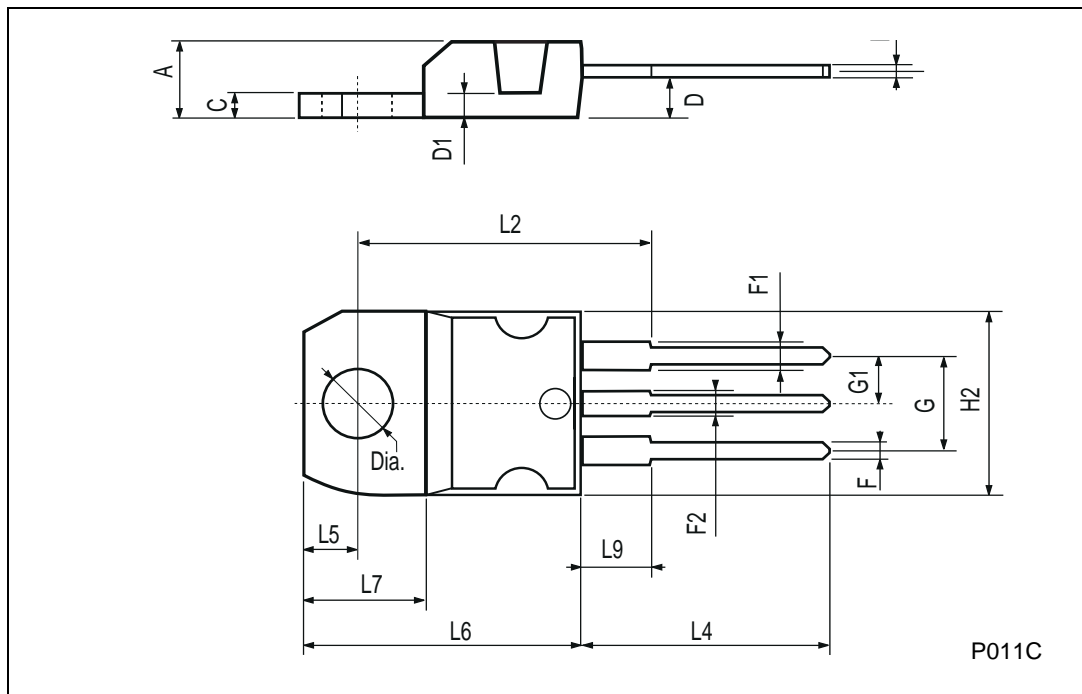


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



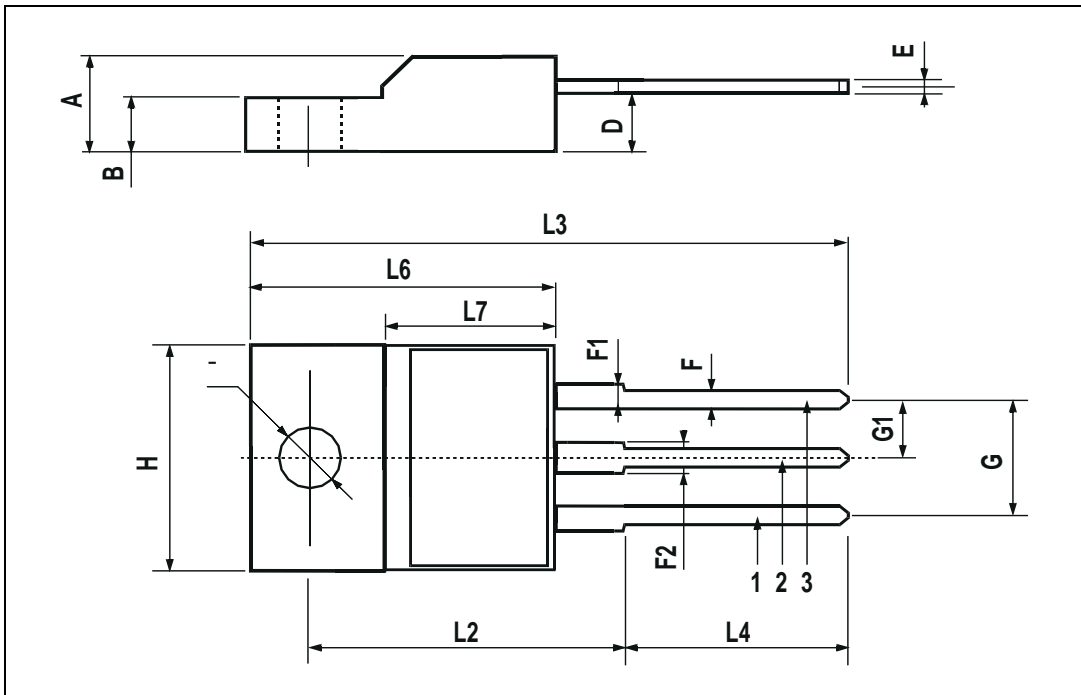
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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