AN1451
APPLICATION NOTE

L6208 FULLY INTEGRATED TWO PHASE STEPPER MOTOR DRIVER

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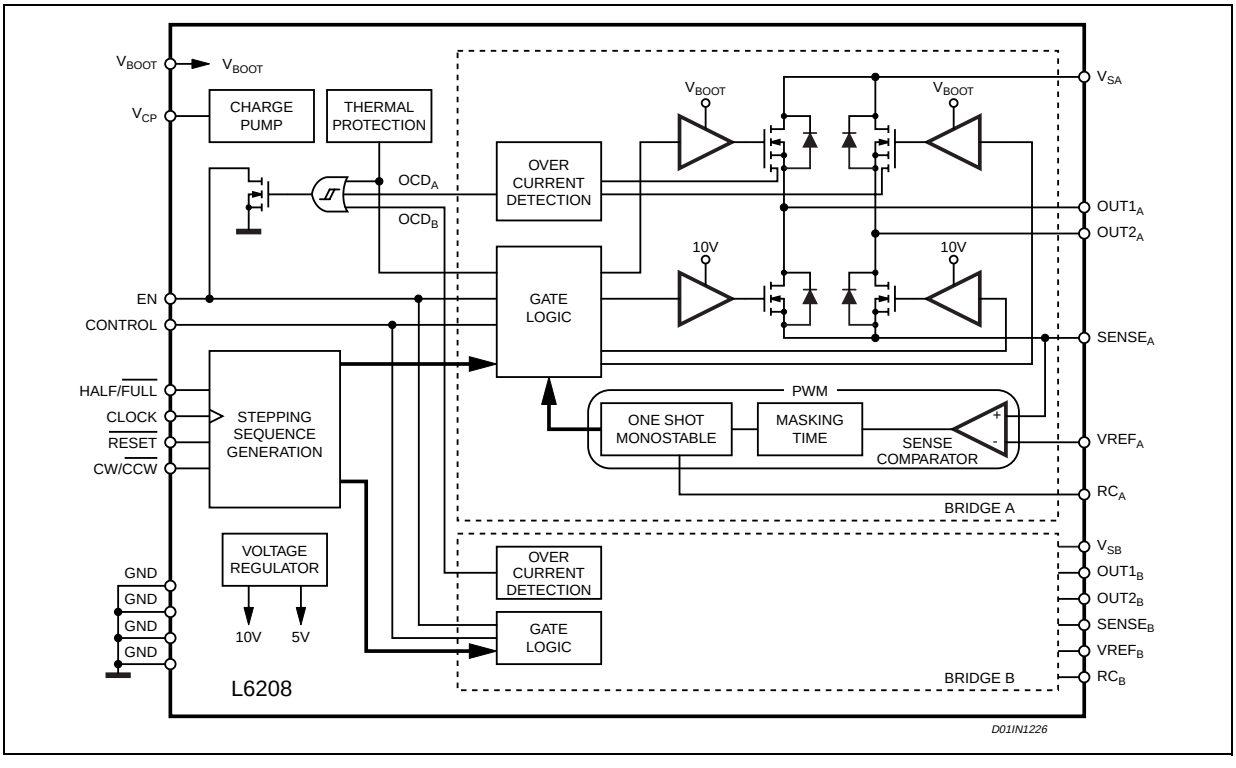
Modern motion control applications need more flexibility that can be addressed only with specialized IC products. The L6208 is a fully integrated stepper motor driver IC specifically developed to drive a wide range of two phase (bipolar) stepper motors. This IC is a one-chip cost effective solution that includes several unique circuit design features. These features, including a decoding logic that can generate three different stepping sequences, allow the device to be used in many applications including microstepping. The principal aim of this development project was to produce an easy to use, fully protected power IC. In addition several key functions such as protection circuit and PWM current control drastically reduce external components count to meet requirements for many different applications.

1 INTRODUCTION

The L6208 is a highly integrated, mixed-signal power IC that allows the user to easily design a complete motor control system for two-phase bipolar stepper motors. Figure 1 shows the L6208 block diagram. The IC integrates eight Power DMOS, a centralized logic circuit which implements the phase generation and a constant t_{OFF} PWM current control technique (*Quasi-Synchronous mode*) for each of the two phases of the motor plus other added features for safe operation and flexibility.

Figure 1. L6208 block diagram.



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2 DESIGNING AN APPLICATION WITH L6208

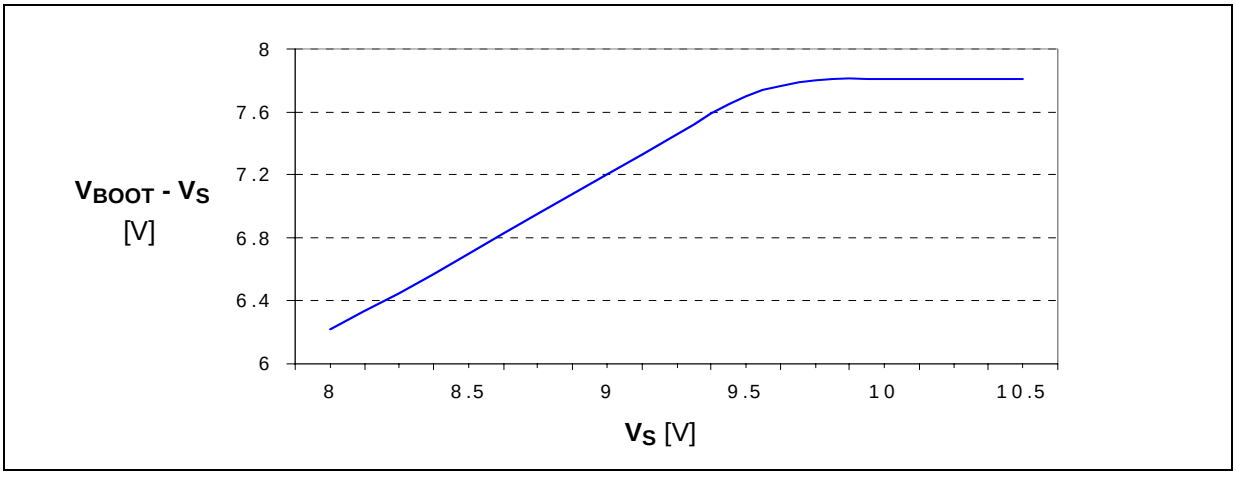
2.1 Current Ratings

With MOSFET (DMOS) devices, unlike bipolar transistors, current under short circuit conditions is, at first approximation, limited by the $R_{DS(ON)}$ of the DMOS themselves and could reach very high values. L6208 *Out* pins and the two V_{SA} and V_{SB} pins are rated for a maximum of 2.8A r.m.s. and 5.6A peak (typical values), corresponding to a total (for the whole IC) 5.6A rms (11.2A peak). These values are meant to avoid damaging metal structures, including the metallization on the die and bond wires. In practical applications, though, maximum allowable current is less than these values, due to power dissipation limits (see *Power Management* section). The device has a built-in Over Current Detection (OCD) that provides protection against short circuits between the outputs and between an output and ground (see *Over Current Protection* section).

2.2 Voltage Ratings and Operating Range

The L6208 requires a single supply voltage (V_S), for the motor supply. Internal voltage regulators provide the 5V and 10V required for the internal circuitry. The operating range for V_S is 8 to 52V. To prevent working into undesirable low supply voltage an *Under Voltage Lock Out* (**UVLO**) circuit shuts down the device when supply voltage falls below 6V; to resume normal operating conditions, V_S must then exceed 7V. The hysteresis is provided to avoid false intervention of the UVLO function during fast V_S ringings. It should be noted, however, that DMOS's $R_{DS(ON)}$ is a function of the V_S supply voltage. Actually, when V_S is less than 10V, $R_{DS(ON)}$ is adversely affected, and this is particularly true for the High Side DMOS that are driven from V_{BOOT} supply. This supply is obtained through a charge pump from the internal 10V supply, which will tend to reduce its output voltage when V_S goes below 10V. Figure 2 shows the supply voltage of the high side gate drivers (V_{BOOT} - V_S) versus the supply voltage (V_S).

Figure 2. High side gate drivers supply voltage versus supply voltage.



Note that V_S must be connected to both V_{SA} and V_{SB} since the bootstrap voltage (at V_{BOOT} pin) is the same for the two H-bridges. The integrated DMOS have a rated Drain-Source breakdown voltage of 60V. However V_S should be kept below 52V, since in normal working conditions the DMOS see a V_{ds} voltage that will exceed V_S supply. In particular, when using the *fast decay* mode, at the beginning of the off-time (when all the DMOS are off during dead-time) the *SENSE* pin sees a negative spike due to a not negligible parasitic inductance of the PCB path from the pin to GND. This spike is followed by a stable negative voltage due to the drop on R_{SENSE}. One of the two *OUT* pins of the bridge sees a similar behavior, but with a slightly larger voltage due to the forward recovery time of the integrated freewheeling diode and the forward voltage drop across it (see Figure 3). Typical duration of this spike is 30ns. At the same time, the other *OUT* pin of the same bridge sees a voltage

above V_S, due to the PCB inductance and voltage drop across the high-side (integrated) freewheeling diode, as the current reverses direction and flows into the bulk capacitor. It turns out that, in fast decay, the highest differential voltage is observed between the two *OUT* pins of the same bridge, at the beginning of the off-time, and this must always be kept below 60V [3]. The same high voltage condition exists when a step is made and the direction of current flow reverses in the bridge.

Figure 3. Currents and voltages during the *dead time* at the beginning of the *off-time*.

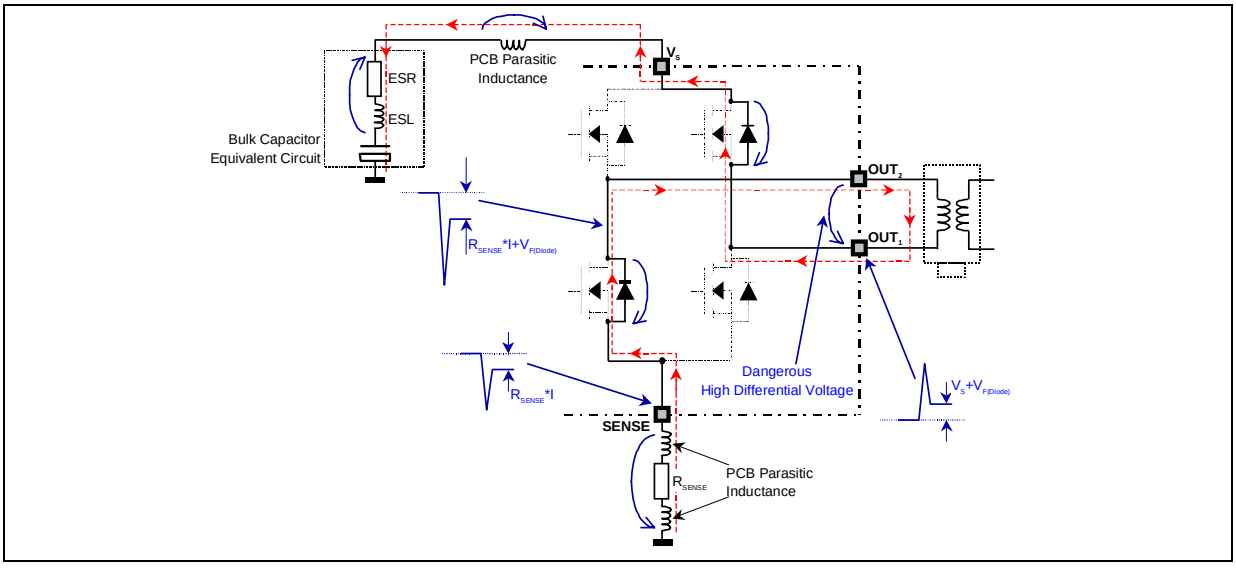
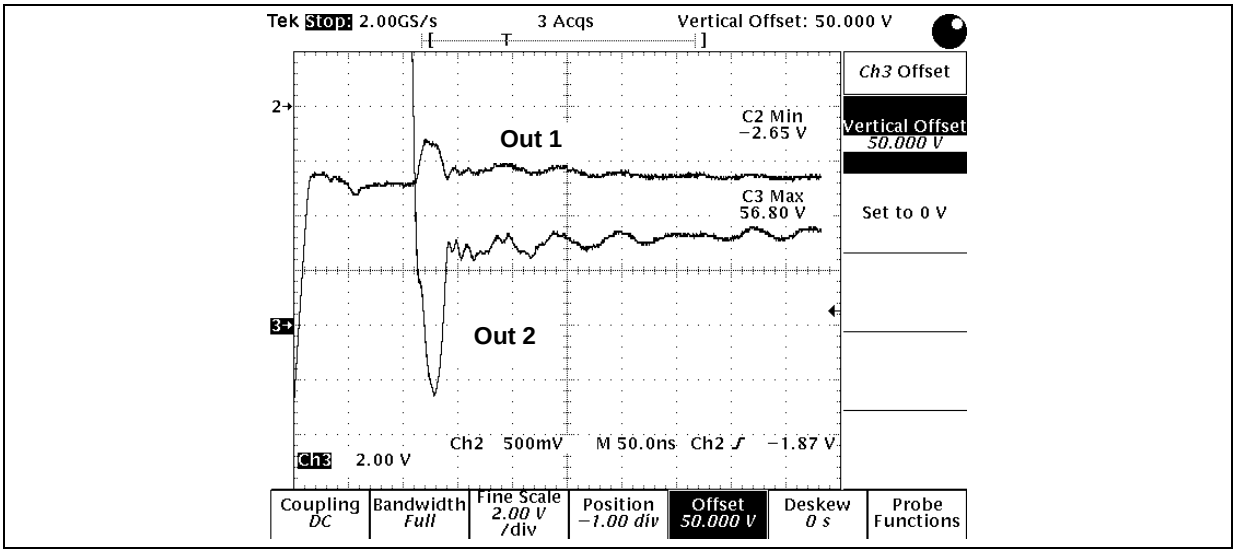


Figure 4 shows the voltage waveforms at the two OUT pins referring to a possible practical situation, with a peak output current of 2.8A, V_S = 52V, R_{SENSE} = 0.33Ω, T_J = 25°C (approximately) and a good PCB layout. Below ground spike amplitude is -2.65V for one output; the other *OUT* pin is at about 57V. In these conditions, total differential voltage reaches almost 60V, which is the absolute maximum rating for the DMOS. Keeping differential voltage between two Output pins belonging to the same Full Bridge within rated values is a must that can be accomplished with proper selection of Bulk capacitor value and equivalent series resistance (ESR), according to current peaks and chopping style and adopting good layout practices to minimize PCB parasitic inductances (see below) [3].

Figure 4. Voltage at the two outputs at the beginning of the off-time.



2.3 Choosing the Bulk Capacitor

Since the bulk capacitor, placed between V_S and *GND* pins, is charged and discharged during IC operation, its **AC current capability** must be greater than the r.m.s. value of the charge/discharge current. This current flows from the capacitor to the IC during the on-time (t_{ON}) and from the IC (in fast decay; from the power supply in slow decay) to the capacitor during the off-time (t_{OFF}). The r.m.s. value of the current flowing into the bulk capacitor depends on peak output current, output current ripple, switching frequency, duty-cycle and chopping style. It also depends on power supply characteristics. A power supply with poor high frequency performances (or long, inductive connections to the IC) will cause the bulk capacitor to be recharged slowly: the higher the current control switching frequency, the higher the current ripple in the capacitor; r.m.s. current in the capacitor, however, does not exceed the r.m.s. output current. Bulk capacitor value (*C*) and the **ESR** determine the amount of voltage ripple on the capacitor itself and on the IC. In slow decay, neglecting the *dead-time* and output current ripple, and assuming that during the *on-time* the capacitor is not recharged by the power supply, the voltage at the end of the *on-time* is:

$$V_S - I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right),$$

so the supply voltage ripple is:

$$I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right),$$

where I_{OUT} is the output current. With fast decay, instead, recirculating current recharges the capacitor, causing the supply voltage to exceed the nominal voltage. This can be very dangerous if the nominal supply voltage is close to the maximum recommended supply voltage (52V). In fast decay the supply voltage ripple is about:

$$I_{OUT} \cdot \left(2 \cdot ESR + \frac{t_{ON} + t_{OFF}}{C} \right),$$

always assuming that the power supply does not recharge the capacitor, and neglecting the output current ripple and the dead-time. Usually (if C > 100 µF) the capacitance role is much less than the ESR, then supply voltage ripple can be estimated as:

$$I_{OUT} \cdot ESR \text{ in slow decay}$$

$$2 \cdot I_{OUT} \cdot ESR \text{ in fast decay}$$

For Example, if a maximum ripple of 500mV is allowed and I_{OUT} = 2A, the capacitor ESR should be lower than:

$$ESR < \frac{0.5V}{2A} = 250m\Omega \text{ in slow decay, and}$$

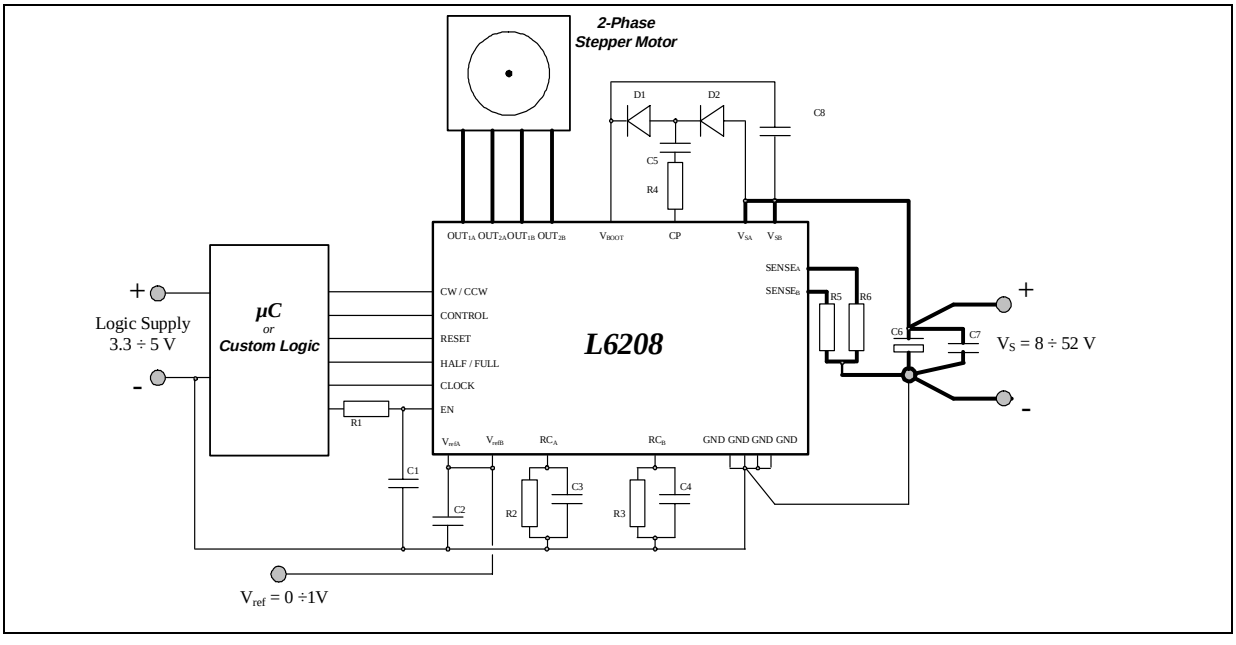
$$ESR < \frac{1}{2} \cdot \frac{0.5V}{2A} = 125m\Omega \text{ in fast decay.}$$

Actually, current sunk by V_{SA} and V_{SB} pins of the device is subject to higher peaks due to reverse recovery charge of internal freewheeling diodes. Duration of these peaks is, tough, very short, and can be filtered using a small value (100÷200 nF), good quality ceramic capacitor, connected as close as possible to the V_{SA}, V_{SB} and GND pins of the IC. Bulk capacitor will be chosen with **maximum operating voltage** 25% greater than the maximum supply voltage, considering also power supply tolerances. For example, with a 48V nominal power supply, with 5% tolerance, maximum voltage is 50.4V, then operating voltage for the capacitor should be at least 63V.

2.4 Layout Considerations

Working with devices that combine high power switches and control logic in the same IC, careful attention has to be paid to the PCB layout. In extreme cases, Power DMOS commutation can induce noises that could cause improper operation in the logic section of the device. Noise can be radiated by high dv/dt nodes or high di/dt paths, or conducted through GND or Supply connections. Logic connections, especially high-impedance nodes (actually all logic inputs, see further), must be kept far from switching nodes and paths. With the L6208, in particular, external components for the charge pump circuitry should be connected together through short paths, since these components are subject to voltage and current switching at relatively high frequency (600kHz). Primary mean in minimizing conducted noise is working on a good GND layout (see Figure 5).

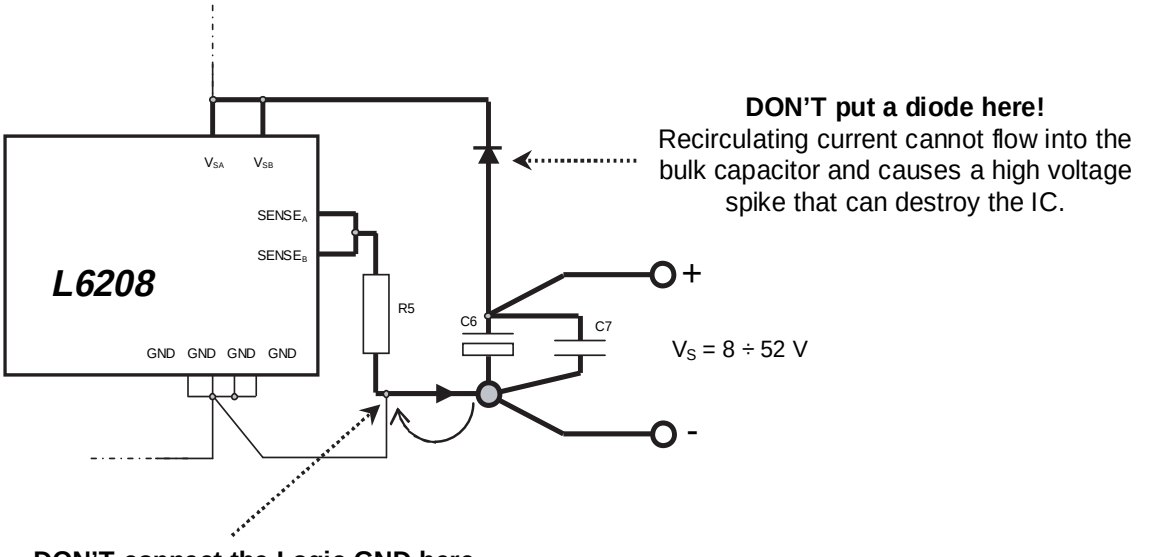
Figure 5. Typical Application and Layout suggestions.



High current GND tracks (i.e. the tracks connected to the sensing resistors) must be connected directly to the negative terminal of the bulk capacitor. A good quality, high-frequency bypass capacitor is also required (typically a 100nF÷200nF ceramic would suffice), since electrolytic capacitors show a poor high frequency performance. Both bulk electrolytic and high frequency bypass capacitors have to be connected with short tracks to V_{SA}, V_{SB} and GND. On the L6208 GND pins are the *Logic* GND, since only the quiescent current flows through them. Logic GND and Power GND should be connected together in a *single point*, the bulk capacitor, to keep noise in the Power GND from affecting Logic GND. Specific care should be paid layouting the path from the *SENSE* pins through the sensing resistors to the negative terminal of the bulk capacitor (Power Ground). These tracks must be as short as possible in order to minimize parasitic inductances that can cause dangerous voltage spikes on *SENSE* and *OUT* pins (see the *Voltage Ratings and Operating Range* section); for the same reason the capacitors on V_{SA}, V_{SB} and GND should be very close to the GND and supply pins. Refer to the Sensing Resistors section for information on selecting the sense resistors. Traces that connect to V_{SA}, V_{SB}, $SENSE_A$, $SENSE_B$, and the four *OUT* pins must be designed with adequate width, since high currents are flowing through these traces, and layer changes should be avoided. Should a layer change prove necessary, multiple and large via holes have to be used. A wide GND copper area can be used to improve power dissipation for the device.

Figure 6 shows two typical situations that must be avoided. An important consideration about the location of the bulk capacitors is the ability to absorb the inductive energy from the load, without allowing the supply voltage to exceed the maximum rating. The diode shown in Figure 6 prevents the recirculation current from reaching the capacitors and will result in a high voltage on the IC pins that can destroy the device. Having a switch or a power connection that can disconnect the capacitors from the IC, while there is still current in the motor, will also result in a high voltage transient since there is no capacitance to absorb the recirculation current.

Figure 6. Two situations that must be avoided.



2.5 Sensing Resistors

Each motor winding current is flowing through the corresponding sensing resistor, causing a voltage drop that is used, by the logic, to control the peak value of the load current. Two issues must be taken into account when choosing the R_{SENSE} value:

– The sensing resistor dissipates energy and provides dangerous negative voltages on the *SENSE* pin during the current recirculation. For this reason the resistance of this component should be kept low.

– The voltage drop across R_{SENSE} is compared with the reference voltage (on V_{ref} pin) by the internal comparator. The lower is the R_{SENSE} value, the higher is the peak current error due to noise on Vref pin and to the input offset of the current sense comparator: too small values of R_{SENSE} must be avoided.

A good compromise is calculating the sensing resistor value so that the voltage drop, corresponding to the peak current in the load (I_{peak}), is about 0.5 V: $R_{SENSE} = 0.5\ V / I_{peak}$.

It should be clear that sensing resistor must absolutely be non-inductive type in order to avoid dangerous negative spikes on *SENSE* pins. Wire-wounded resistors cannot be used here, while Metallic film resistors are recommended for their high peak current capability and low inductance. For the same reason the connections between the *SENSE* pins, C6, C7, V_{SA}, V_{SB} and *GND* pins (see Figure 5) must be taken as short as possible (see also the *Layout Considerations* section).

The average power dissipated by the sensing resistor is:

Fast Decay Recirculation: $P_R \approx I_{rms}^2 \cdot R_{SENSE}$

Slow Decay Recirculation: $P_R \approx I_{rms}^2 \cdot R_{SENSE} \cdot D$,

D is the duty-cycle of the PWM current control, I_{rms} is the r.m.s. value of the load current.

Nevertheless, sensing resistor power rating should be chosen taking into account the peak value of the dissipated power:

$$P_R \approx I_{pk}^2 \cdot R_{SENSE} \quad ,$$

where I_{pk} is the peak value of the load current.

Using multiple resistors in parallel will help obtaining the required power rating with standard resistors, and reduce the inductance.

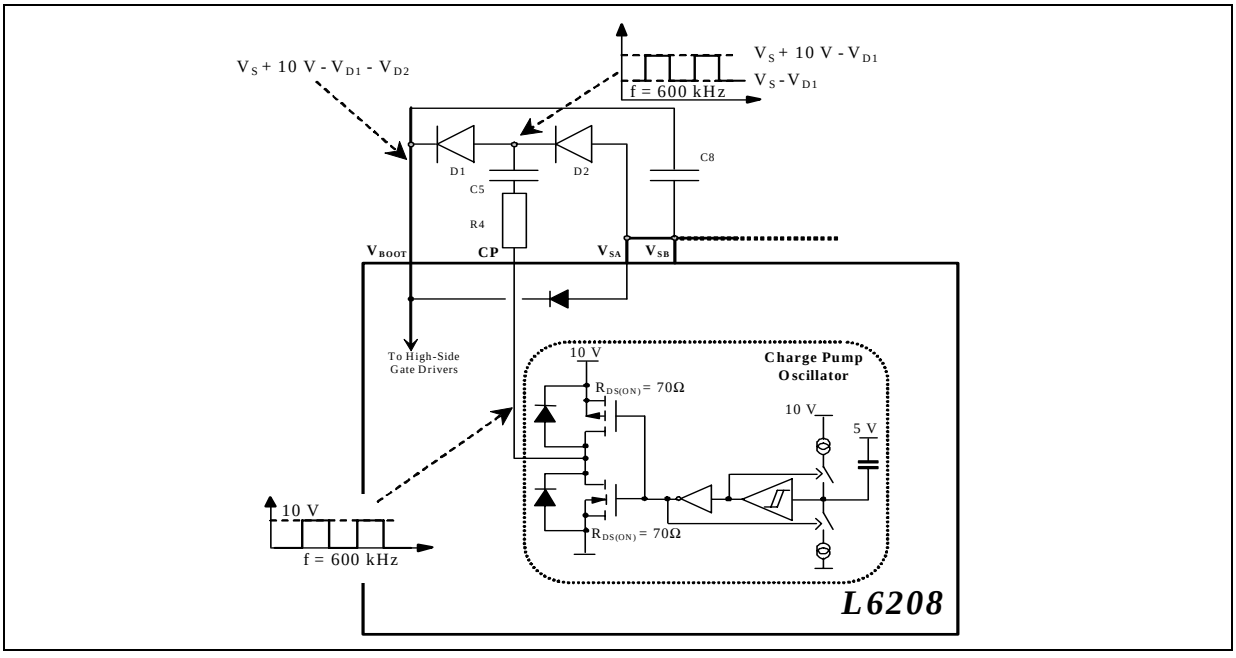
R_{SENSE} tolerance reflects on the peak current error: 1% resistors should be preferred.
The following table shows R_{SENSE} recommended values (to have 0.5V drop on it) and power ratings for typical examples of current peak values.

I_{pk}	R_{SENSE} Value [Ω]	R_{SENSE} Power Rating [W]	Alternatives
0.5	1	0.25	
1	0.5	0.5	2 X 1Ω, 0.25W paralleled
1.5	0.33	0.75	3 X 1Ω, 0.25W paralleled
2	0.25	1	4 X 1Ω, 0.25W paralleled

2.6 Charge pump external components

An internal oscillator, with its output at *CP* pin, switches from GND to 10V with a typical frequency of 600kHz (see Figure 7).

Figure 7. Charge Pump.



When the oscillator output is at ground, C_5 is charged by V_S through D_2. When it rises to 10V, D_2 is reverse biased and the charge flows from C_5 to C_8 through D_1, so the V_{BOOT} pin, after a few cycles, reaches the maximum voltage of V_S + 10V - V_{D1} - V_{D2}, which supplies the high-side gate drivers.

With a differential voltage between V_S and V_{BOOT} of about 9V and both the bridges switching at 50kHz, the typical current drawn by the V_{BOOT} pin is 1.85 mA.

Resistor *R4* is added to reduce the maximum current in the external components and to reduce the slew rate of the rising and falling edges of the voltage at the *CP* pin, in order to minimize interferences with the rest of the circuit. For the same reason care must be taken in realizing the PCB layout of *R4*, *C5*, *D1*, *D2* connections (see also the *Layout Considerations* section). Recommended values for the charge pump circuitry are:

D1, D2 : 1N4148

R4 : 100 Ω (1/8 W)

C5 : 10nF 100V ceramic

C8 : 220nF 25V ceramic

Due to the high charge pump frequency, fast diodes are required. Connecting the cold side of the bulk capacitor (C8) to V_S instead of GND the average current in the external diodes during operation is less than 10 mA (with R4 = 100 Ω); at startup (when V_S is provided to the IC) is less than 200 mA while the reverse voltage is about 10 V in all conditions. 1N4148 diodes withstand about 200 mA DC (1 A peak), and the maximum reverse voltage is 75 V, so they should fit for the majority of applications.

2.7 Sharing the Charge Pump Circuitry

If more than one device is used in the application, it's possible to use the charge pump from one L6208 to supply the V_{BOOT} pins of several ICs. The unused *CP* pins on the slaved devices are left unconnected, as shown in Figure 8. A 100nF capacitor (C8) should be connected to the V_{BOOT} pin of each device.

Supply voltage pins (V_S) of the devices sharing the charge pump must be connected together.

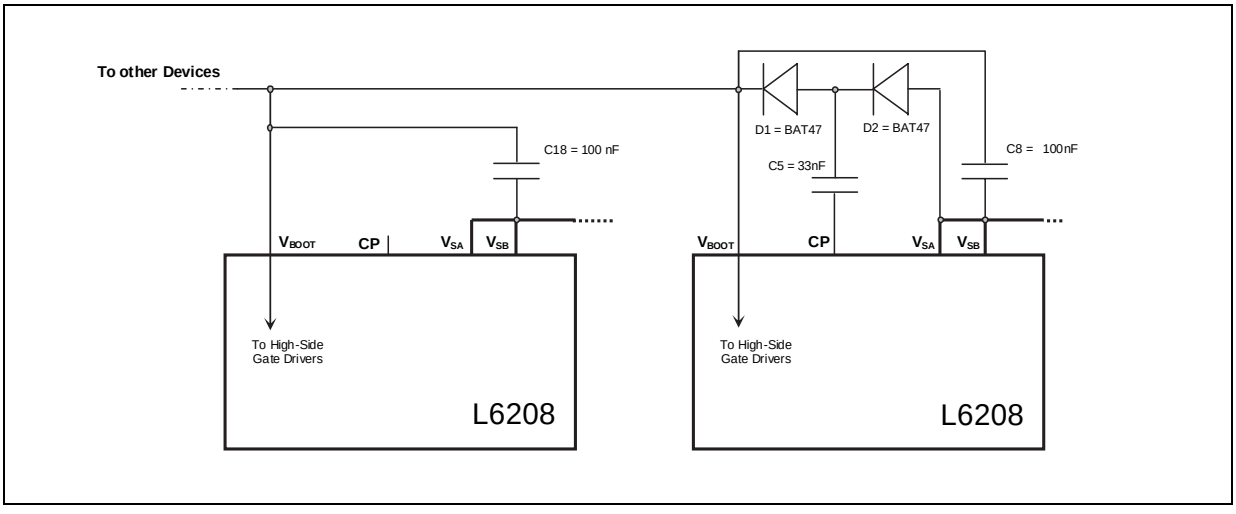
The higher the number of devices sharing the same charge pump, the lower will be the differential voltage available for gate drive (V_{BOOT} - V_S), causing a higher $R_{DS(ON)}$ for the high side DMOS, so higher dissipating power.

In this case it's recommended to omit the resistor on the *CP* pin, obtaining a higher current capability of the charge pump circuitry.

Better performance can also be obtained using a 33nF capacitor for C5 and using schottky diodes (for example BAT47 are recommended).

Sharing the same charge pump circuitry for more than 3÷4 devices is not recommended, since it will reduce the V_{BOOT} voltage increasing the high-side MOS on-resistance and thus power dissipation.

Figure 8. Sharing the charge pump circuitry.



2.8 Reference Voltage for PWM Current Control

The device has two analog inputs, V_{refA} and V_{refB}, connected to the internal sense comparators, to control the peak value of the motor current through the integrated PWM circuitry. In typical applications these pins are connected together, in order to obtain the same current in the two motor windings (one exception is the microstepping operation; see the related section). A fixed reference voltage can be easily obtained through a resistive divider from an available 5 V voltage rail (maybe the one supplying the µC or the rest of the application) and GND.

A very simple way to obtain a variable voltage without using a DAC is to low-pass filter a PWM output of a µC (see Figure 9).

Assuming that the PWM output swings from 0 to 5V, the resulting voltage will be:

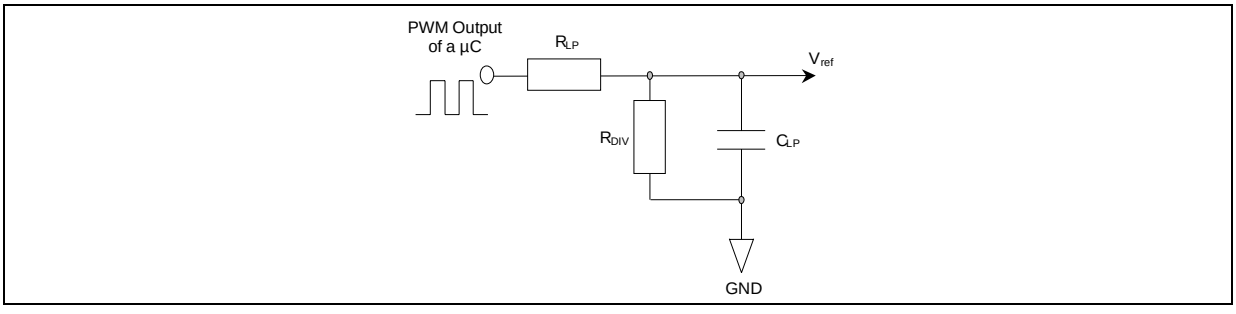
$$V_{ref} = \frac{5V \cdot D_{\mu C} \cdot R_{DIV}}{R_{LP} + R_{DIV}}$$

where $D_{\mu C}$ is the duty-cycle of the PWM output of the µC.

Assuming that the µC output impedance is lower than 1kΩ, with R_{LP} = 56kΩ, R_{DIV} = 15kΩ, C_{LP} = 10nF and a µC PWM switching from 0 to 5V at 100kHz, the low pass filter time constant is about 0.12 ms and the remaining ripple on the V_{ref} voltage will be about 20 mV. Using higher values for R_{LP}, R_{DIV} and C_{LP} will reduce the ripple, but the reference voltage will take more time to vary after changing the duty-cycle of the µC PWM, and too high values of R_{LP} will also increase the impedance of the V_{ref} net at low frequencies, causing a poor noise immunity.

As sensing resistor values are typically kept small, a small noise on V_{ref} input pins might cause a considerable error in the output current. It's then recommended to decouple these pins with ceramic capacitors of some tens of nF, placed very close to V_{ref} and GND pins. Note that V_{ref} pins cannot be left unconnected, while, if connected to GND, zero current is not guaranteed due to voltage offset in the sense comparator. The best way to cut down (IC) power consumption and clear the load current is pulling down the *EN* pin. In slow decay, with very small reference voltage, PWM integrated circuitry can loose control of the current due to the minimum allowed duration of t_{ON} (see the *Programmable off-time Monostable* section).

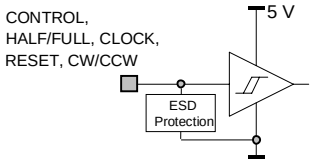
Figure 9. Obtaining a variable voltage through a PWM output of a µC.



2.9 Input Logic pins

CW/CCW, CONTROL, RESET, HALF/FULL, CLOCK are CMOS/TTL compatible logic input pins. The input comparator has been realized with hysteresis to ensure the required noise immunity. Typical values for turn-on and turn-off thresholds are $V_{th,ON}$ = 1.8V and $V_{th,OFF}$ = 1.3V. Pins are ESD protected (see Figure 10) (2kV human-body electrostatic discharge), and can be directly connected to the logic outputs of a µC; a series resistor is generally not recommended, as it could help inducted noise to disturb the inputs. All logic pins enforce a specific behavior and cannot be left unconnected.

Figure 10. Logic input pins.

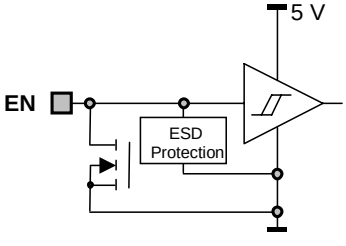


2.10 EN pin

The EN pin is, actually, bi-directional: as an input, with a comparator similar to the other logic input pins (TTL/CMOS with hysteresis), it controls the state of the PowerDMOS. When this pin is at a low logic level, all the PowerDMOS are turned off. The EN pin is also connected to the open drain output of the protection circuit that will pull the pin to GND if over current or over temperature conditions exist. For this reason, EN pin must be driven through a series resistor of 2.2kΩ minimum (for 5V logic), to allow the voltage at the pin to be pulled below the turn-off threshold.

A capacitor (C1 in Figure 5) connected between the EN pin and GND is also recommended, to reduce the r.m.s. value of the output current when overcurrent conditions persist (see *Over Current Protection* section). EN pin must not be left unconnected.

Figure 11. EN input pin.



2.11 Programmable off-time Monostable

The L6208 includes a constant off time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOS transistors and ground, as shown in Figure 12. As the current in the motor builds up the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$) the sense comparator triggers the monostable switching the bridge off. The power MOS remain off for the time set by the monostable and the motor current recirculates as defined by the selected decay mode, described in the next section. When the monostable times out the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time is the sum of the monostable time plus the dead time.

Figure 12. PWM Current Controller Simplified Schematic

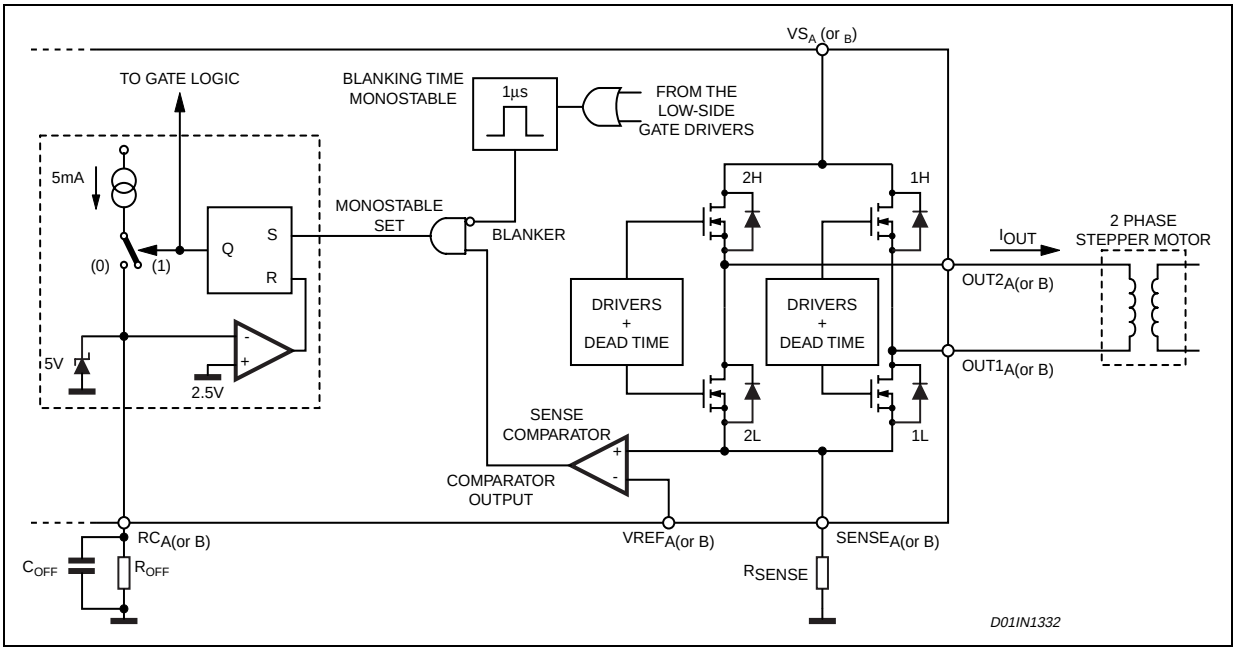


Figure 13 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. More details regarding the Synchronous Rectification and the output stage configuration are included in the next section.

Immediately after the Power MOS turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6208 provides a 1µs Blanking Time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 13. Output Current Regulation Waveforms

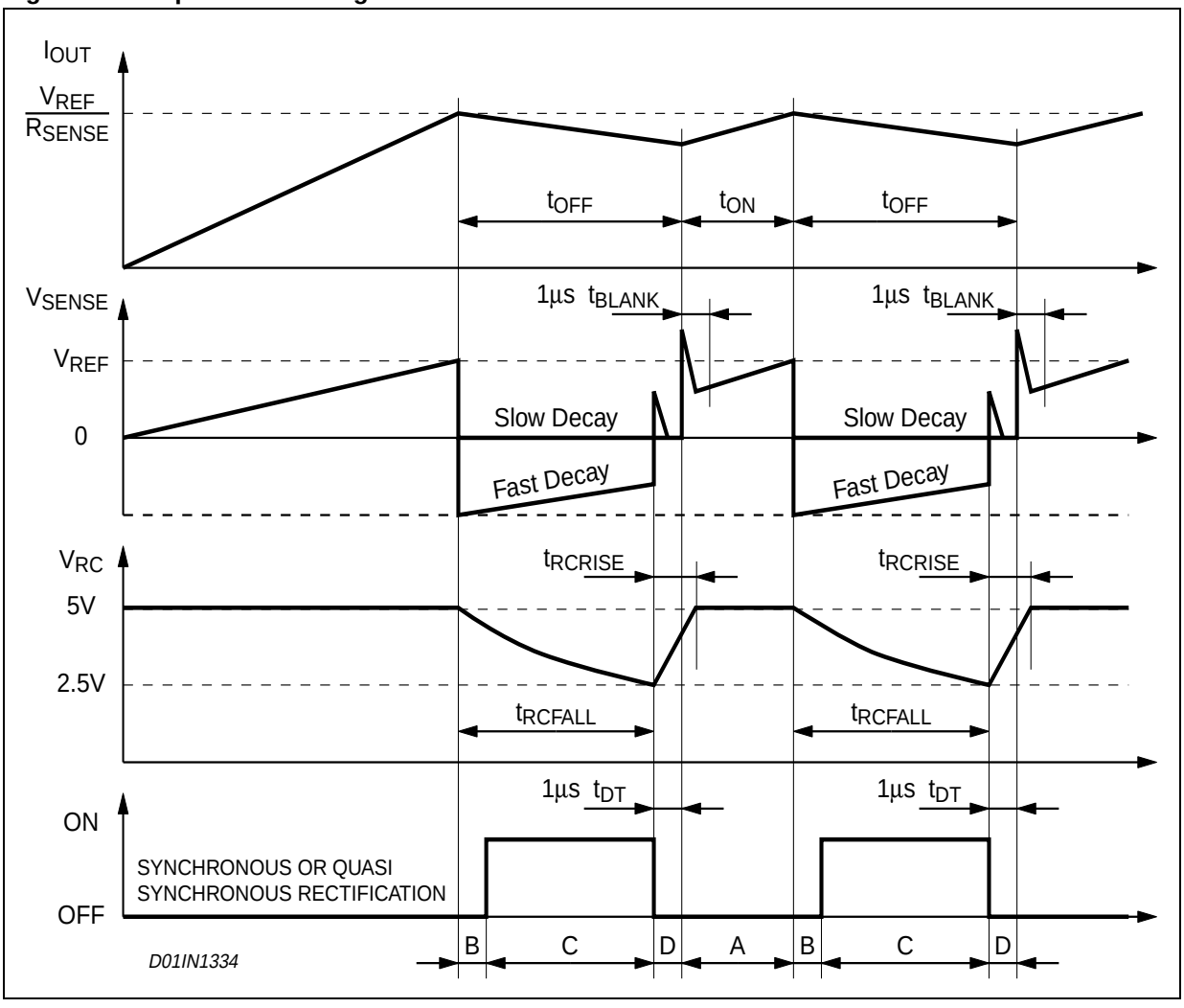


Figure 14 shows the magnitude of the Off Time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$

$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$20K\Omega \leq R_{OFF} \leq 100K\Omega$

$0.47nF \leq C_{OFF} \leq 100nF$

$t_{DT} = 1\mu s$ (typical value)

Therefore:

$t_{OFF(MIN)} = 6.6\mu s$

$t_{OFF(MAX)} = 6ms$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the Rise Time t_{RCRISE} of the voltage at the pin RC_A (or RC_B). The Rise Time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON}, which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON}

can not be smaller than the minimum on time $t_{ON(MIN)}$.

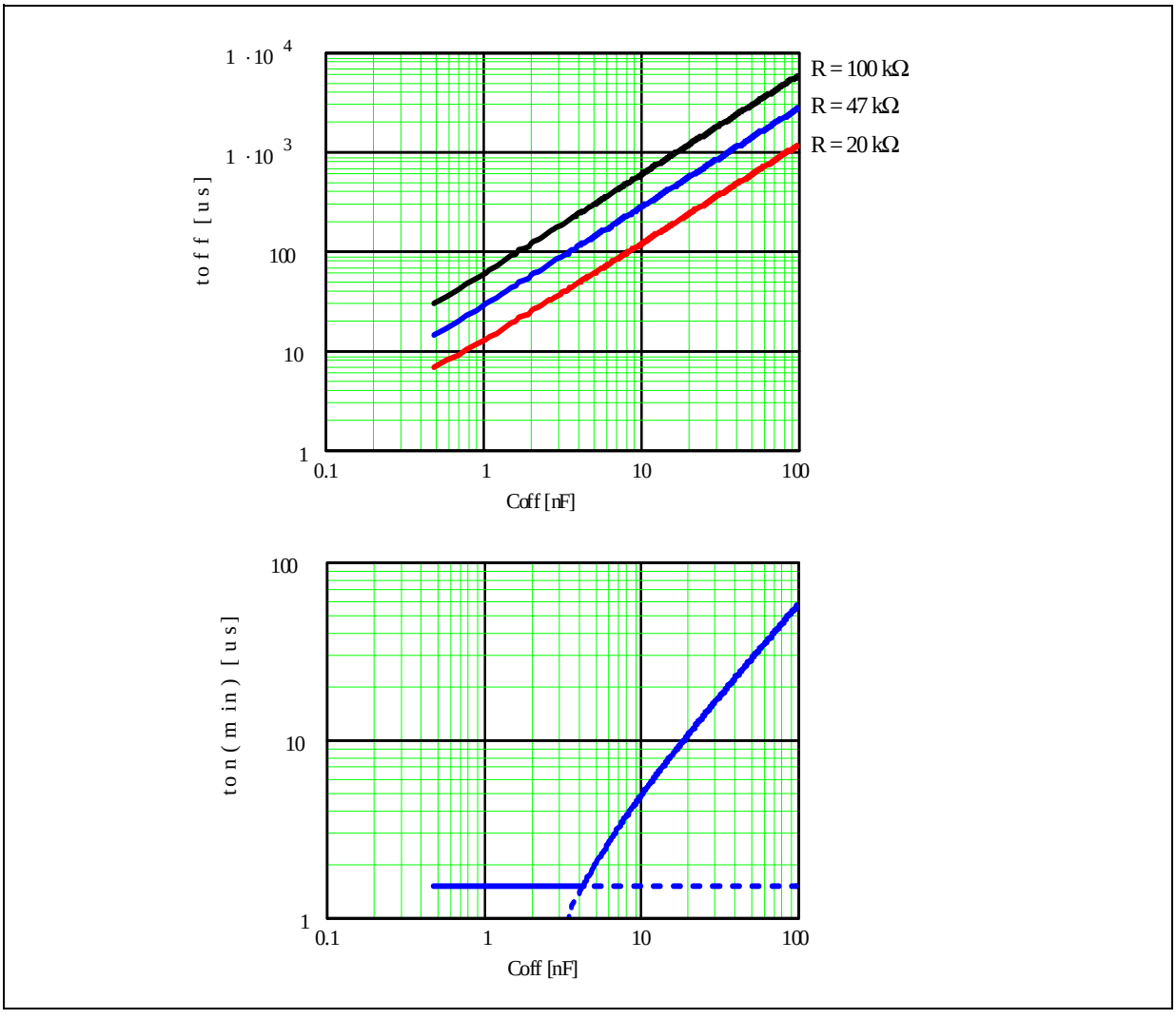
$$\begin{cases} t_{ON} > t_{ON(MIN)} = 1.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

2.11.1 Off-time Selection and minimum on-time

Figure 14 also shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the off time t_{OFF} is not more constant.
So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 14. Off-time selection and minimum on-time.



2.11.2 Decay Modes

The CONTROL input is used to select the behavior of the bridge during the off time. When the CONTROL pin is low, the Fast Decay mode is selected and both transistors in the bridge are switched off during the off time. When the CONTROL pin is high, the Slow Decay mode is selected and only the low side transistor of the bridge is switched off during the off time.

Figure 15 shows the operation of the bridge in the Fast Decay mode. At the start of the off time, both of the power MOS are switched off and the current recirculates through the two opposite free wheeling diodes. The current decays with a high di/dt since the voltage across the coil is essentially the power supply voltage. After the dead time, the lower power MOS in parallel with the conducting diode is turned on in synchronous rectification mode. In applications where the motor current is low it is possible that the current can decay completely to zero during the off time. At this point if both of the power MOS were operating in the synchronous rectification mode it would then be possible for the current to build in the opposite direction. To prevent this only the lower power MOS is operated in synchronous rectification mode. This operation is called Quasi-Synchronous Rectification Mode. When the monostable times out, the power MOS are turned on again after some delay set by the dead time to prevent cross conduction.

Figure 16 shows the operation of the bridge in the Slow Decay mode. At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the dead time the upper power MOS is operated in the synchronous rectification mode. When the monostable times out, the lower power MOS is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 15. Fast Decay Mode Output Stage Configurations

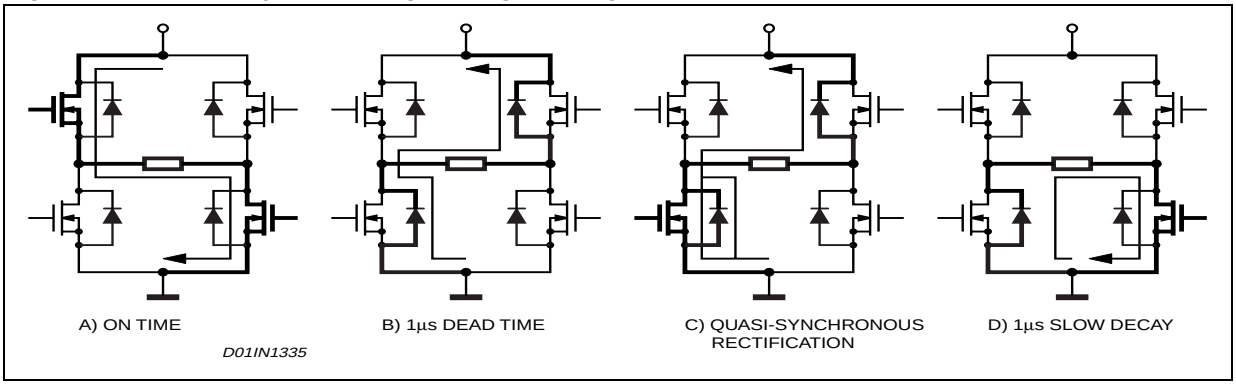
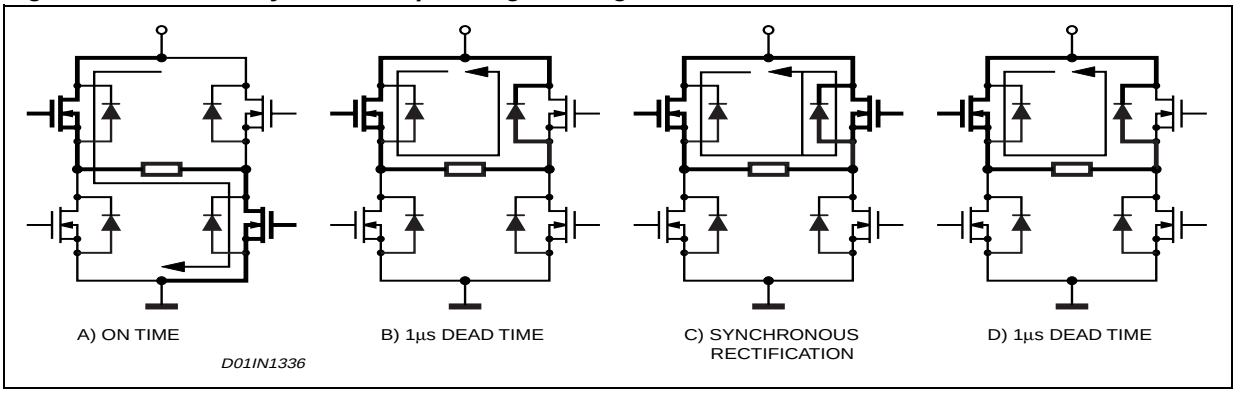


Figure 16. Slow Decay Mode Output Stage Configurations



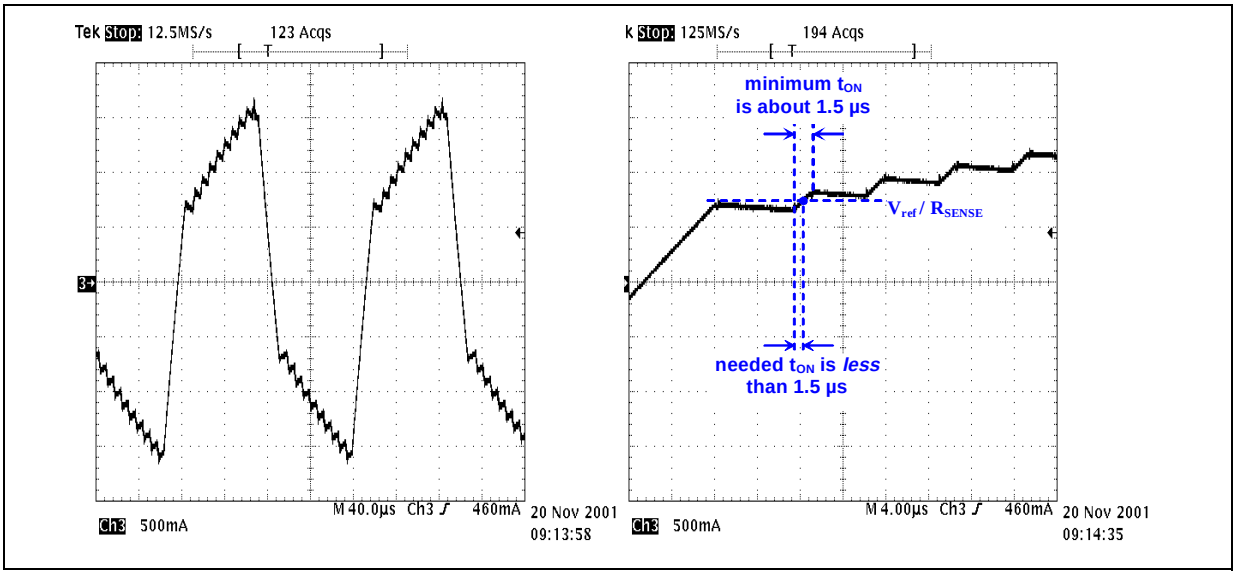
In some conditions (short off-time, very low regulated current, high motor winding L / R) the system may need an on-time shorter than 1.5µs. In these cases the PWM current controller can loose the regulation.

Figure 17 shows the operation of the circuit in this condition. When the current first reaches the threshold, the bridge is turned off for a fixed time and the current decays. During the following on-time current increases above the threshold, but the bridge cannot be turned off until the minimum 1.5µs on-time expires. Since current increases more in each on-time than it decays during the off-time, it keeps growing during each cycle, with steady state asymptotic value set by duty-cycle and load DC resistance: the resulting peak current will be

$I_{pk} = V_S \cdot D / R_{LOAD}$,

where $D = t_{ON} / (t_{ON} + t_{OFF})$ is the duty-cycle and R_{LOAD} is the load DC resistance.

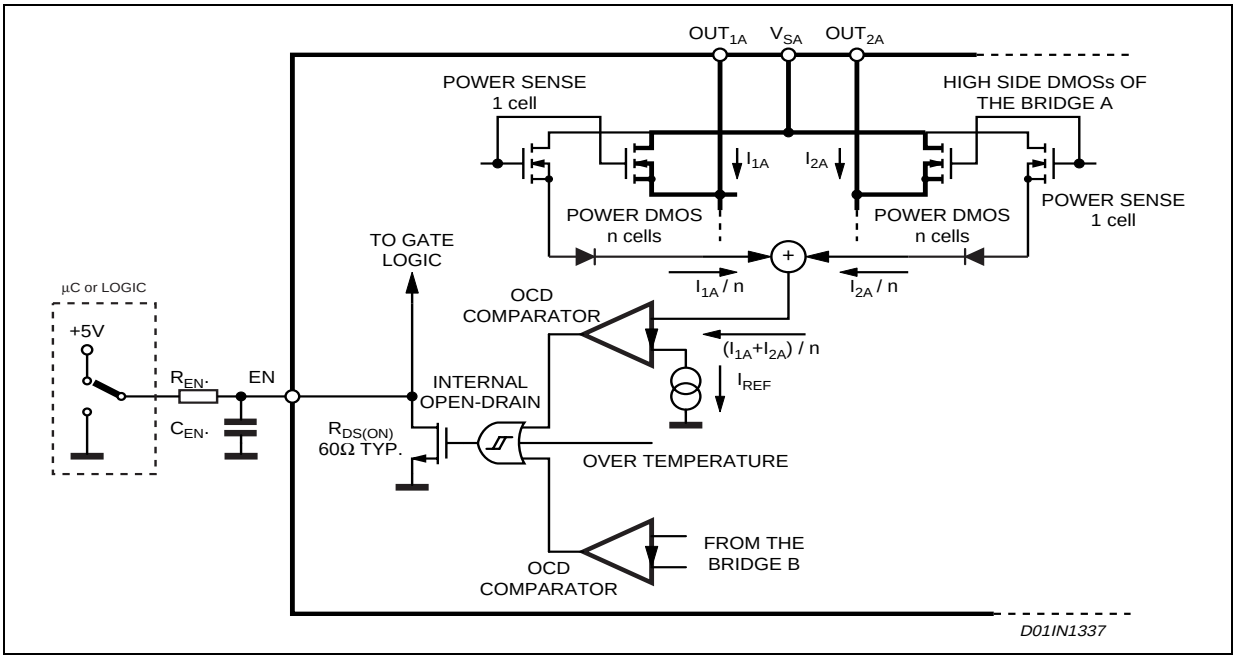
Figure 17. Minimum on-time can cause the PWM controller to loose the regulation.



2.12 Over Current Protection

To implement an Over Current (i.e. short circuit) Protection, a dedicated Over Current Detection (OCD) circuitry (see Figure 18 for a simplified schematic) senses the current in each high side. Power DMOS are actually made up with thousands of individual identical cells, each carrying a fraction of the total current flowing. The current sensing element, connected in parallel to the Power DMOS, is made only with few such cells, having a 1:N ratio compared to the power DMOS. The total drain current is split between the output and the sense element according to the cell ratio. Sensed current is, then, a small fraction of the output current and will not contribute significantly to power dissipation.

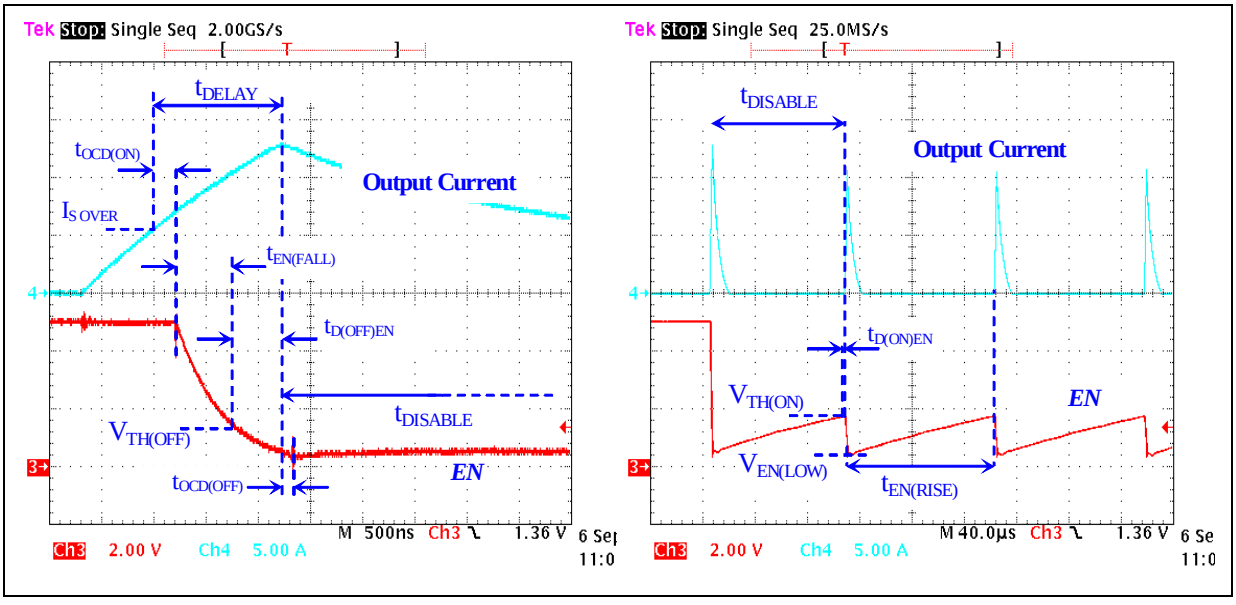
Figure 18. Over Current Detection simplified circuitry.



This sensed current is compared to an internally generated reference to detect an over current condition. An internal open drain mosfet turns on when the sum of the currents in the bridges 1A and 2A or 1B and 2B reaches the threshold (5.6A typical value); the open drain is internally connected to the *EN* pin. To ensure an over current protection, connect this pin to an external RC network (see Figure 18).

Figure 19 shows the device operating in overcurrent condition (short to ground). When an over current is detected the internal open drain mosfet pulls the *EN* pin to GND switching off all 8 power DMOS of the device and allowing the current to decay. Under a persistent over current condition, like a short to ground or a short between two output pins, the external RC network on the *EN* pin (see Figure 18) reduces the r.m.s. value of the output current by imposing a fixed disable-time after each over current occurrence. The values of R_{EN} and C_{EN} are selected to ensure proper operation of the device under a short circuit condition. When the current flowing through the high side DMOS reaches the OCD threshold (5.6 A typ.), after an internal propagation delay ($t_{OCD(ON)}$) the open drain starts discharging C_{EN}. When the *EN* pin voltage falls below the turn-off threshold ($V_{TH(OFF)}$) all the Power DMOS turn off after the internal propagation delay ($t_{D(OFF)EN}$). The current begins to decay as it circulates through the freewheeling diodes. Since the DMOS are *off*, there is no current flowing through them and no current to sense so the OCD circuit, after a short delay ($t_{OCD(OFF)}$), switches the internal open drain device off, and R_{EN} can charge C_{EN}. When the voltage at *EN* pin reaches the turn-on threshold ($V_{TH(ON)}$), after the $t_{D(ON)EN}$ delay, the DMOS turn on and the current restarts. Even if the maximum output current can be very high, the external RC network provides a disable time ($t_{DISABLE}$) to ensure a safe r.m.s. value (see Figure 19).

Figure 19. Over Current Operation.



The maximum value reached by the current depends on its slew-rate, so on the short circuit nature and supply voltage, and on the total intervention delay (t_{DELAY}). It can be noticed that after the first current peak, the maximum value reached by the output current becomes lower, because the capacitor on *EN* pin is discharged starting from a lower voltage, resulting in a shorter t_{DELAY}.

The following approximate relations estimate the disable time and the first OCD intervention delay after the short circuit (worst case).

The time the device remains disabled is:

$$t_{DISABLE} = t_{OCD(OFF)} + t_{EN(RISE)} + t_{D(ON)EN}$$

where

$$t_{EN(RISE)} = R_{EN} \cdot C_{EN} \cdot \ln \frac{V_{DD} - V_{EN(LOW)}}{V_{DD} - V_{TH(ON)}}$$

$V_{EN(LOW)}$ is the minimum voltage reached by the *EN* pin, and can be estimated with the relation:

$$V_{EN(LOW)} = V_{TH(OFF)} \cdot e^{\frac{t_{D(OFF)EN} + t_{OCD(OFF)}}{R_{OPDR} \cdot C_{EN}}}$$

The total intervention time is

$$t_{DELAY} = t_{OCD(ON)} + t_{EN(FALL)} + t_{D(OFF)EN}$$

where

$$t_{EN(FALL)} = R_{OPDR} \cdot C_{EN} \cdot \ln \frac{V_{DD}}{V_{TH(OFF)}}$$

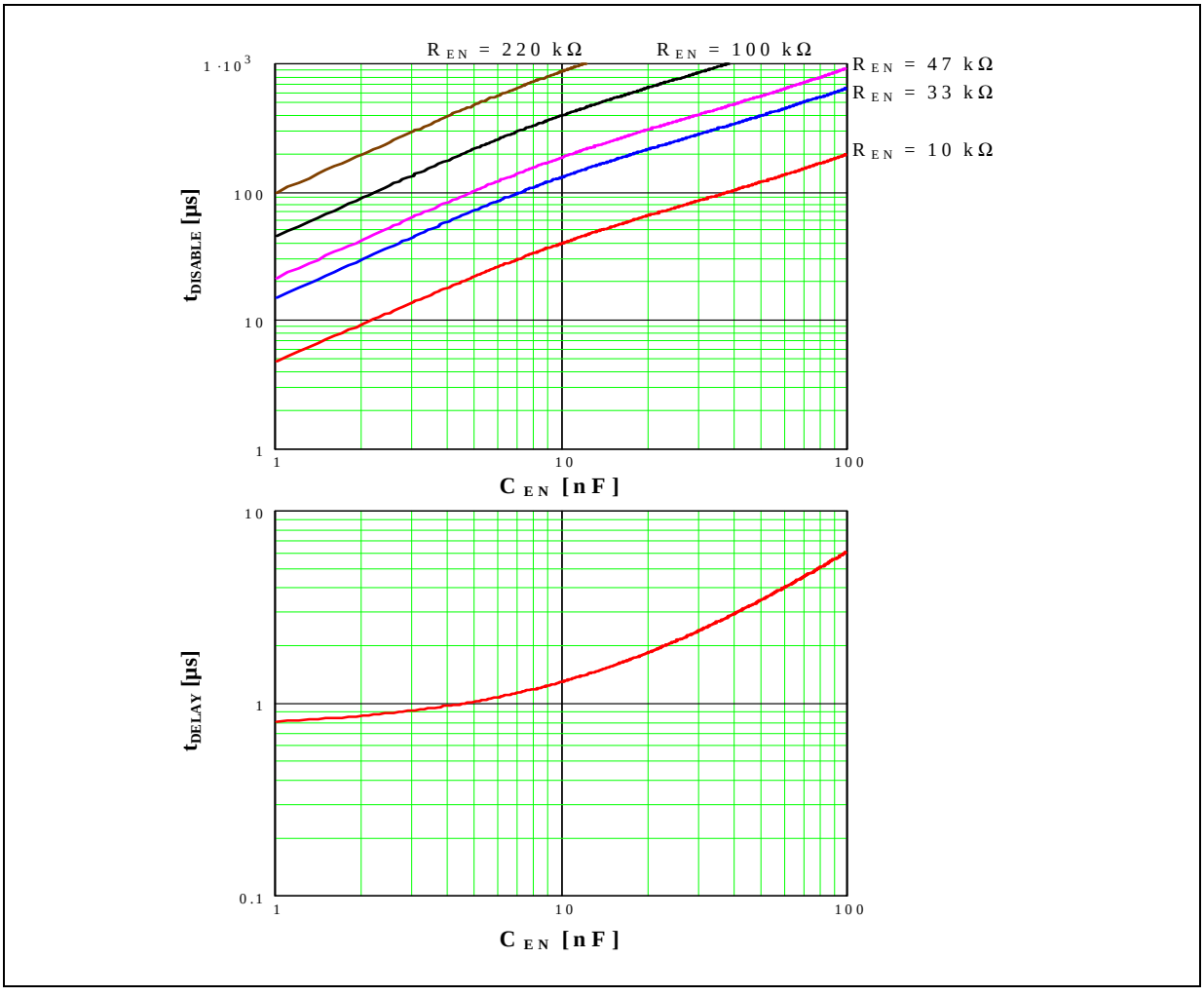
$t_{OCD(OFF)}$, $t_{OCD(ON)}$, $t_{D(ON)EN}$, $t_{D(OFF)EN}$, and R_{OPDR} are device intrinsic parameters, V_{DD} is the pull-up voltage

applied to R_{EN}.

The external RC network, C_{EN} in particular, must be chosen obtaining a reasonable fast OCD intervention (short t_{DELAY}) and a safe disable time (long $t_{DISABLE}$). Figure 20 shows both $t_{DISABLE}$ and t_{DELAY} as a function of C_{EN}: at least 100µs for $t_{DISABLE}$ are recommended, keeping the delay time below 1÷2µs at the same time.

The internal open drain can also be turned on if the device experiences an **over temperature** (OVT) condition. The OVT will cause the device to shut down when the die temperature exceeds the OVT threshold (T_J>165 °C typ.). Since the OVT is also connected directly to the gate drive circuit (see Figure 1), all the Power DMOS will shut down, even if *EN* pin voltage is still over $V_{th(OFF)}$. When the junction temperature falls below the OVT turn-off threshold (150 °C typ.), the open drain turns off, C_{EN} is recharged up to $V_{TH(ON)}$ and then the PowerDMOS are turned on back.

Figure 20. Typical disable and delay time as a function of C_{EN}, for several values of R_{EN}.

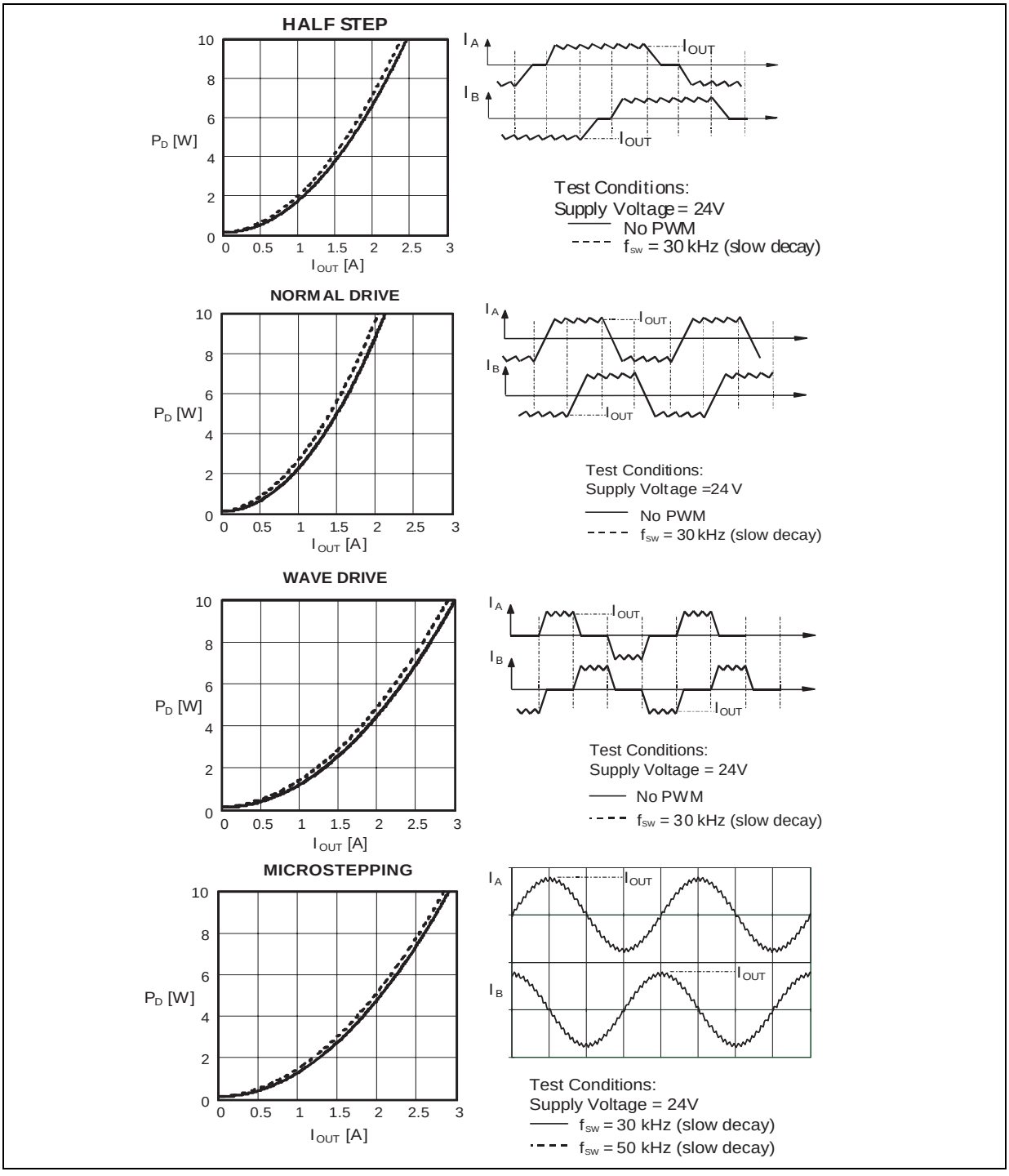


2.13 Power Management

Even when operating at current levels well below the maximum ratings of the device, the operating junction temperature must be kept below 125 °C.

Figure 21 shows the IC dissipated power versus the r.m.s. load current, in 4 different driving sequences, assuming the supply voltage is 24V.

Figure 21. IC Dissipated Power versus Output Current.

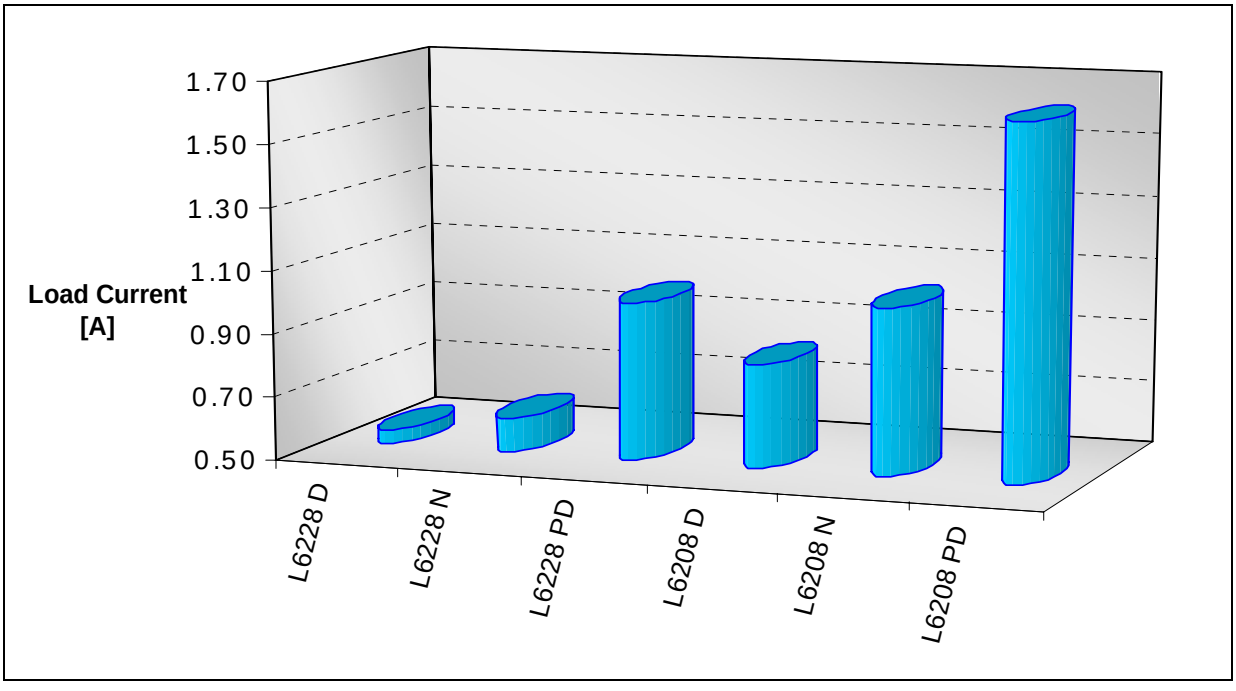


2.13.1 Maximum output current vs. selectable devices

Figure 22 reports a performance comparison between L6228 (std. power) and L6208 (high power) for different packages, with the following assumptions:

- Normal Drive Mode (two-phase on)
- Supply voltage: 24 V; Switching frequency: 30 kHz.
- T_{amb} = 25 °C, T_J = 125 °C.
- Maximum $R_{DS(ON)}$ (taking into account process spread) has been considered, @ 125 °C.
- Maximum quiescent current I_Q (taking into account process spread) has been considered.
- PCB is a FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm) for SO and PowerDIP packages (D, N suffixes).
- PCB is a FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer for the PowerSO package (PD suffix).
- For each device (on the x axis) y axis reports the maximum output current.

Figure 22. Maximum output current vs. selectable devices.



2.13.2 Power Dissipation Formulae for different sequences

Figure 23 to Figure 26 are screenshots of a spreadsheet that helps calculating power dissipation in specified conditions (application and motor data), and estimates the resulting junction temperature for a given package and copper area available on the PCB [6]. The model considers power dissipation during the on-time and the off-time, taking into account the selected decay, rise and fall time (when a phase change occurs) considering the operating sequence, the switching losses and the quiescent current power dissipation.

Figure 23. Definition of parameters for the three different sequences. The current in only one phase is shown.

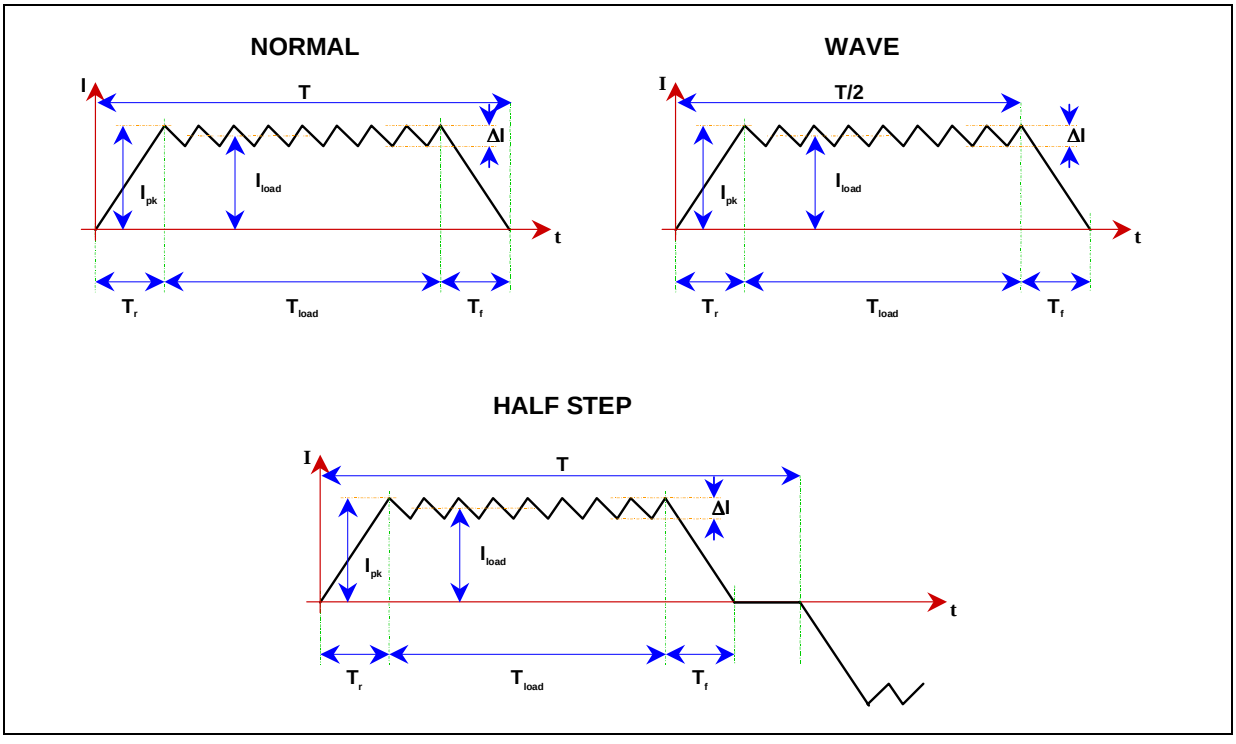


Figure 24. Input Data.

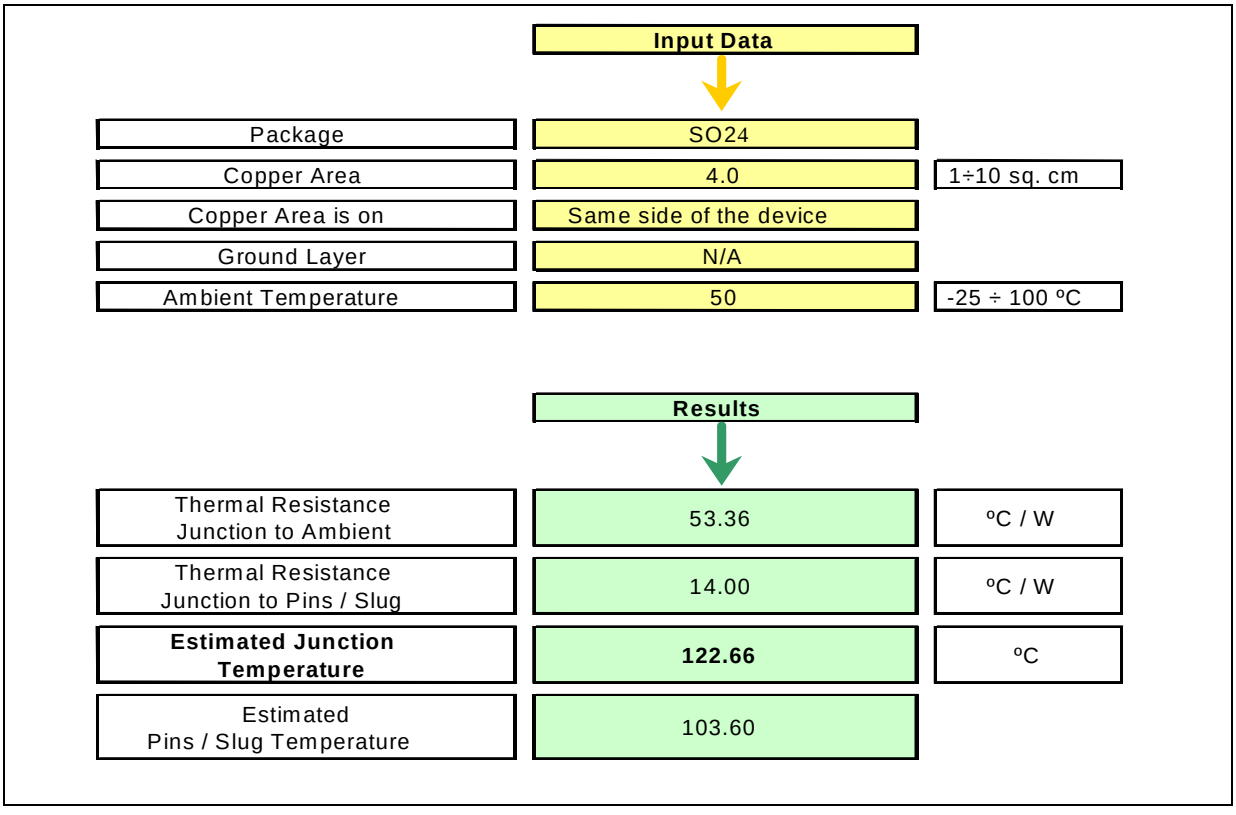
Input Data

Device Input Values				
Maximum Drain-Source ON Resistance	Ron	= 5.60E-01	[Ohm]	Average Value between High-Side and Low-Side
Maximum diode voltage	Vd	= 1.20E+00	[V]	
Quiescent Current	Iq	= 5.50E-03	[mA]	
Motor Input Values				
Maximum BEMF Voltage	Vb	= 1.50E+01	[V]	
Motor Inductance	Lm	= 7.90E-03	[H]	
Motor Resistance	Rm	= 6.60E+00	[Ohm]	
Application Input Values				
Supply Voltage	Vs	= 2.40E+01	[V]	
Peak Current	Ipk	= 1.00E+00	[A]	
Off-Time	tOFF	= 1.50E-05	[s]	
Step Frequency	fCK	= 1.00E+03	[Hz]	
Sensing Resistance	Rs	= 5.00E-01	[Ohm]	
Decay Type	SLOW		-	"SLOW" = Synchronous Slow Decay "FAST" = Quasi-Synchronous Fast decay
Stepping sequence	WAVE		-	"NORMAL", "HALF" or "WAVE"

Figure 25. Power Dissipation formulae and results.

		Result			
PowerDMOS Commutation Time	Tcom =	9.60E-08	[s]	Vs / (250V/µs)	
Rise Time	Trise =	4.03E-04	[s]	$-\ln\left[\frac{(-Ipk\cdot Rm-2\cdot Ipk\cdot Ron-Ipk\cdot Rs+Vs)}{Vs}\right]\cdot\frac{Lm}{Rm+Rs+2Ron}$	
Fall Time	Tfall =	3.16E-04	[s]	$-\ln\left[\frac{Vs}{(Ipk\cdot Rm+2\cdot Ipk\cdot Ron+Ipk\cdot Rs+Vs)}\right]\cdot\frac{Lm}{(Rm+2\cdot Ron+Rs)}$ $-\ln\left[\frac{(Vs-2\cdot Vd)}{(Ipk\cdot Rm+Ipk\cdot Rs+Vs-2\cdot Vd)}\right]\cdot\frac{Lm}{(Rm+Rs)}$	NORMAL Mode HALF or WAVE Mode
Duty Cycle	D =	6.25E-01	-	Vb / Vs (Vs + Vb) / 2Vs	Sync. Slow Decay Quasi-Sync Fast Decay
Switching Frequency	fSW =	2.50E+04	[Hz]	(1-D) / tOFF	
Current Ripple	ΔI =	2.85E-02	[A]	(Vs - Vb)*D / (Lm* fSW)	
Period	T =	2.00E-03	[s]	2 / fCK 4 / fCK 2 / fCK	NORMAL Mode HALF Mode WAVE Mode
Load Time	Tload =	5.97E-04	[s]	T-Trise-Tfall (3/4)T-rise (T/2)-Trise	NORMAL Mode HALF Mode WAVE Mode
Average Current during Load Time	I =	9.86E-01	[A]	$Ipk-\frac{\Delta I}{2}$	
r.m.s. Current during Load Time	Irms =	9.86E-01	[A]	$\sqrt{Ipk\cdot(Ipk-\Delta I)+\frac{\Delta I^2}{3}}$	
Rise Time Dissipating Energy	Erise =	1.50E-04	[J]	$2Ron\cdot Ipk^2\cdot\frac{Trise}{3}$	
Fall Time Dissipating Energy	Efall =	3.62E-04	[J]	$2Ron\cdot Ipk^2\cdot\frac{Tfall}{3}$ $2\cdot Vd\left[Tfall\cdot\frac{(-Vs+2\cdot Vd)}{(Rm+Rs)}+Lm\cdot(Ipk\cdot Rm+Ipk\cdot Rs+Vs-2\cdot Vd)\cdot\frac{\left[1-\exp\left[\frac{-Tfall}{Lm}\cdot(Rm+Rs)\right]\right]}{(Rm+Rs)^2}\right]$	MORMAL Mode HALF or WAVE Mode
Load Time Diss. Energy	Eload =	6.50E-05	[J]	$2Ron\cdot Irms^2\cdot Tload$ $2Ron\cdot Irms^2\cdot D\cdot Tload + (Ron\cdot Irms^2 + Vd\cdot I)\cdot(1-D)\cdot Tload$	Sync. Slow Decay Quasi-Sync Fast Decay
Commutatiion Time Dissipating Pw	Ecom =	6.78E-05	[J]	$2Vs\cdot I\cdot Tcom\cdot Tload\cdot fSW$	
Quiescent Dissipating Pw	Pq =	1.32E-01	[W]	$Vs\cdot Iq$	
Total Dissipating Power	**P =**	**1.36E+00**	**[W]**	$\frac{2}{T}\cdot(Erise+Efall+Eload+Ecom)+Pq$	

Figure 26. Thermal Data inputs and results.



2.14 Choosing the Decay Mode

L6208 can operate in either fast or slow decay mode, each having a specific recirculation path for the current during off-time. In slow decay mode only the lower DMOS is turned off and the current recirculates around the upper half of the bridge so that voltage across the coil is essentially 0. In Fast decay mode both DMOS are turned off and the current recirculates back to the power supply rail so that voltage across the coil is essentially power supply voltage itself.

Slow decay operation provides several advantages: for a given peak current and off-time, current ripple is minimized, and the same is true for acoustic noise and losses in the motor iron (achieving the same current ripple with fast decay mode would require a shorter off-time resulting in a higher switching frequency and higher power dissipation in the IC). As current recirculates in the upper half of the bridge and both the high side DMOS in the same bridge are on, *synchronous* rectification is realized, minimizing power dissipation in the power switches. Also, as no output pin goes below GND (see *Supply Voltage Ratings and Operating Range* section), no power is dissipated on the sense resistor during the off-time (see *Sensing Resistors* section).

On the other hand, slow decay can be undesirable in some situations, for example when current has to be regulated at very low values or motor winding L / R ratio is high. In these cases an on-time shorter than the minimum t_{ON} (about 1.5µs) may be requested to regulate the current, and this can cause the PWM controller to loose the regulation (refer to the *Programmable off-time Monostable* section).

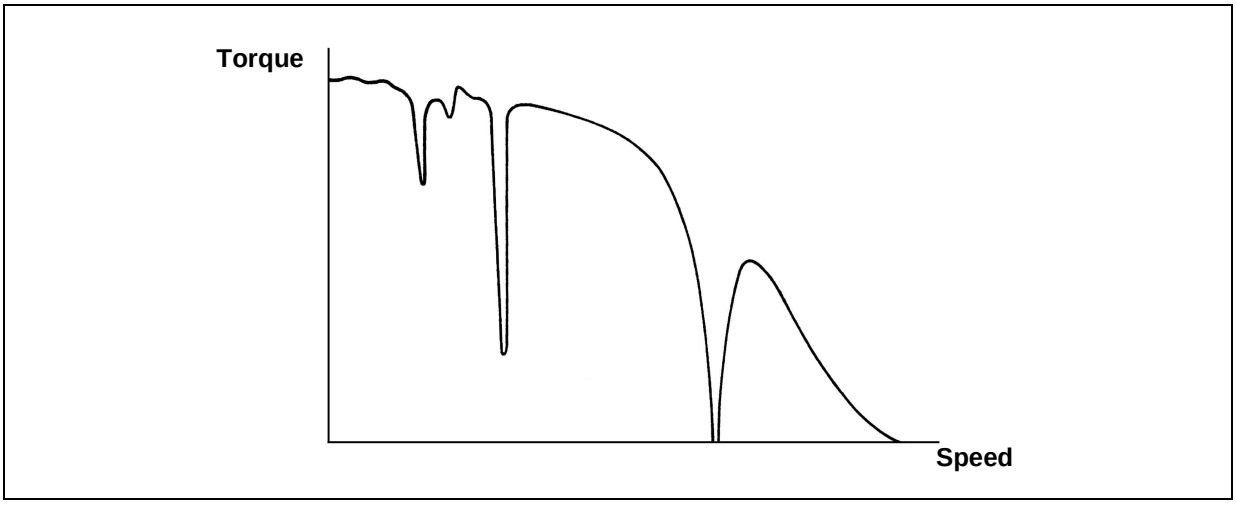
Another situation where fast decay is to be preferred to slow decay is with regulated current expected to vary over time with a given profile (enforced providing a variable voltage on the V_{ref} pins, see also *Microstepping* section). Here fast decay helps following fast decreasing edges in the desired profile.

2.15 Choosing the Stepping Sequence

The device can provide three different sequences to run a stepper motor: full step two phase on (Normal drive), full step one phase on (Wave drive) and Half step.

If *Half Step* driving is used, the motor advances by half a step after each clock pulse, obtaining a higher position resolution and reducing instability due to low-torque regions in certain motors' speed-torque diagrams, when used in full step mode (see Figure 27).

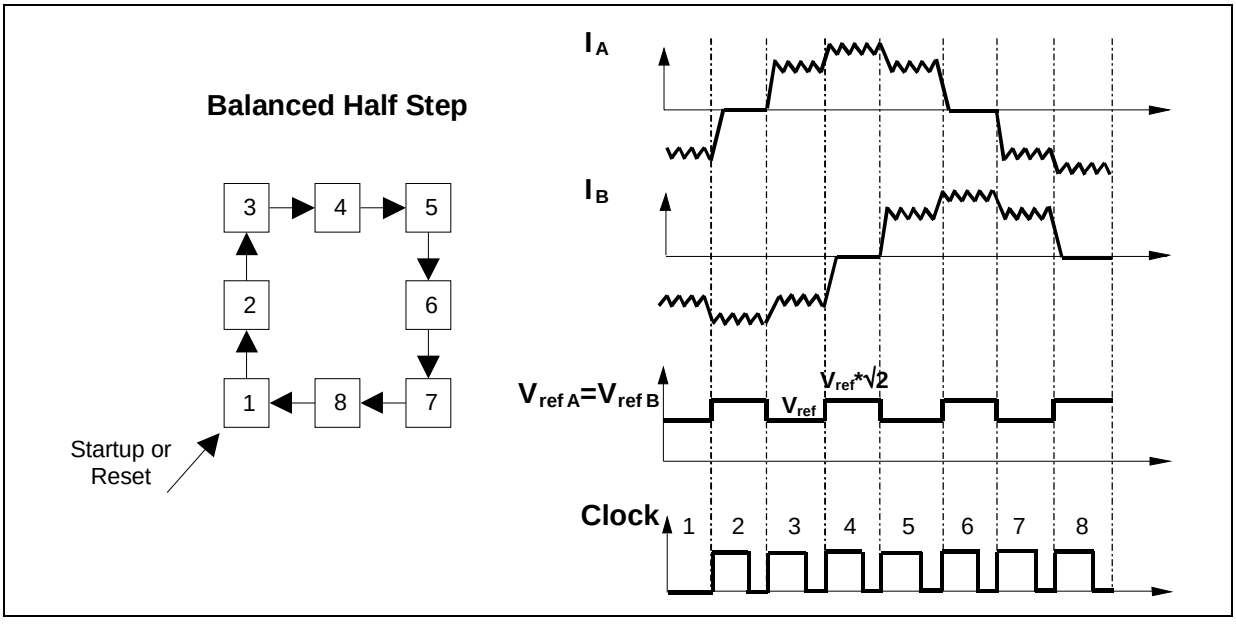
Figure 27. Torque instability in full step mode.



Using this driving method the torque is affected by ripple, because in odd-numbered states, when both coils are driven, the total current in the motor windings is double than in even-numbered states.

A way to avoid the high torque ripple in half step mode is to supply to the motor a higher current (by a factor of $\sqrt{2}$) during the even numbered states, in which only one winding is energized, simply by applying a $\sqrt{2}$ higher reference voltage at the V_{refA}, V_{refB} pins during these states (see Figure 28) [2].

Figure 28. Balanced Half Step for low torque ripple.



A simple circuit to generate two different reference voltages is shown in Figure 29. R_1 and R_2 should be chosen to have

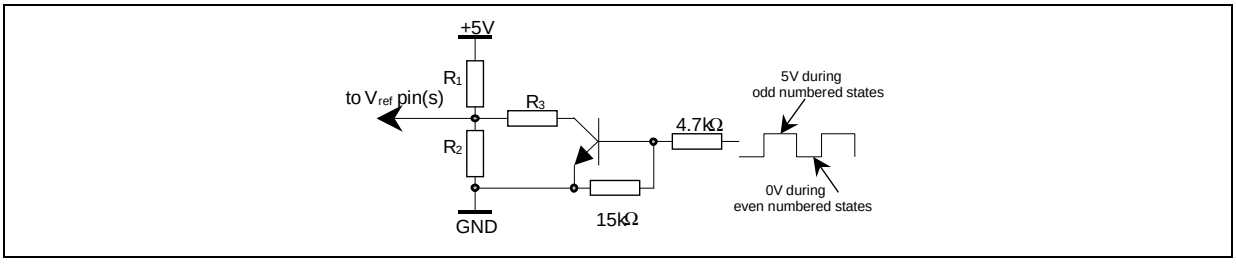
$$V_{ref,\,HIGH} = V_{ref} \cdot \sqrt{2} = 5V \cdot \frac{R_2}{R_1 + R_2}$$

and R_3 should be

$$R_3 = \frac{R_1 \cdot R_2}{(\sqrt{2} - 1) \cdot (R_1 + R_2)}$$

A similar circuit can also be used to modify the reference voltage in other situations. For example it's possible, at constant rotation speed, to reduce the motor torque, and to increase it during acceleration and deceleration. Adding a second transistor is possible to implement 4 different reference voltages, selectable by two logic signals.

Figure 29. Realizing Half Step current shaping.



Normal and Wave Drive are full step modes. In Wave Drive mode the two motor windings are alternately energized, while in Normal Drive both the windings are energized in each state, increasing the torque by a factor of $\sqrt{2}$. On the other hand the total current in the motor is double, so the efficiency is similar. In wave drive mode the torque ripple is higher than in normal drive mode.

2.16 Microstepping

Microstepping operation gives several advantages, including the absence of instability phenomena due to low-torque regions in certain motors' speed-torque diagrams (see Figure 27), reduction of mechanical noise and increased position resolution. The L6208 can be used as two-phase microstepping driver IC [5]. The controller circuitry allows for an easy and inexpensive design with such device. By controlling the V_{ref} input it is possible to get in the two phases variable output currents with a sine-wave shape. A variable voltage proportional to the desired output current is applied to each reference pin. For microstepping, the two inputs are rectified sine-wave voltages with a phase delay of 90°. The L6208 is operated in the normal drive mode and the frequency of the two sine-wave voltages must be 1/4 of the CLOCK frequency. Figure 30 shows a circuit to generate the two sine-wave signals using low-pass filters and two PWM outputs of a µC (see *Reference Voltage for PWM Current Control* section). Figure 31 shows the V_{ref} voltages, the CLOCK signal and the output currents.

Figure 30. Microstepping Application.

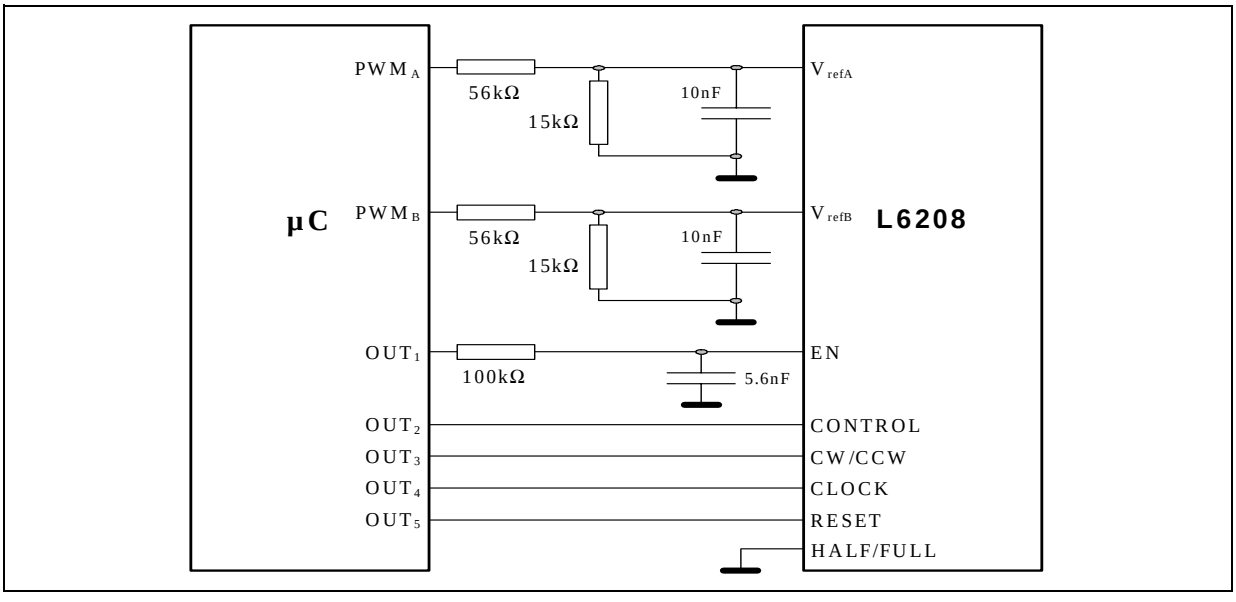
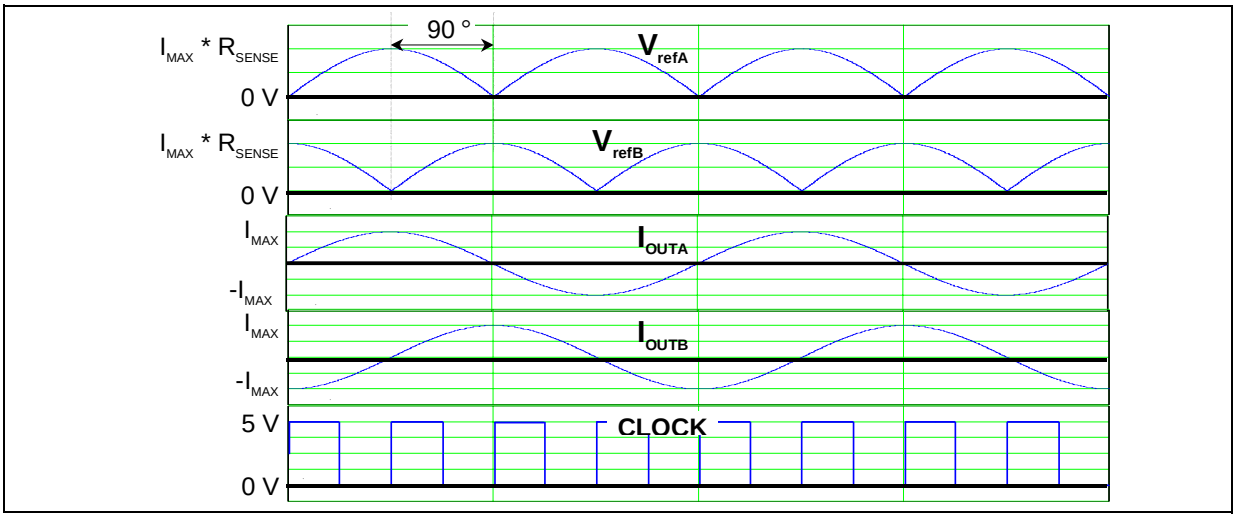
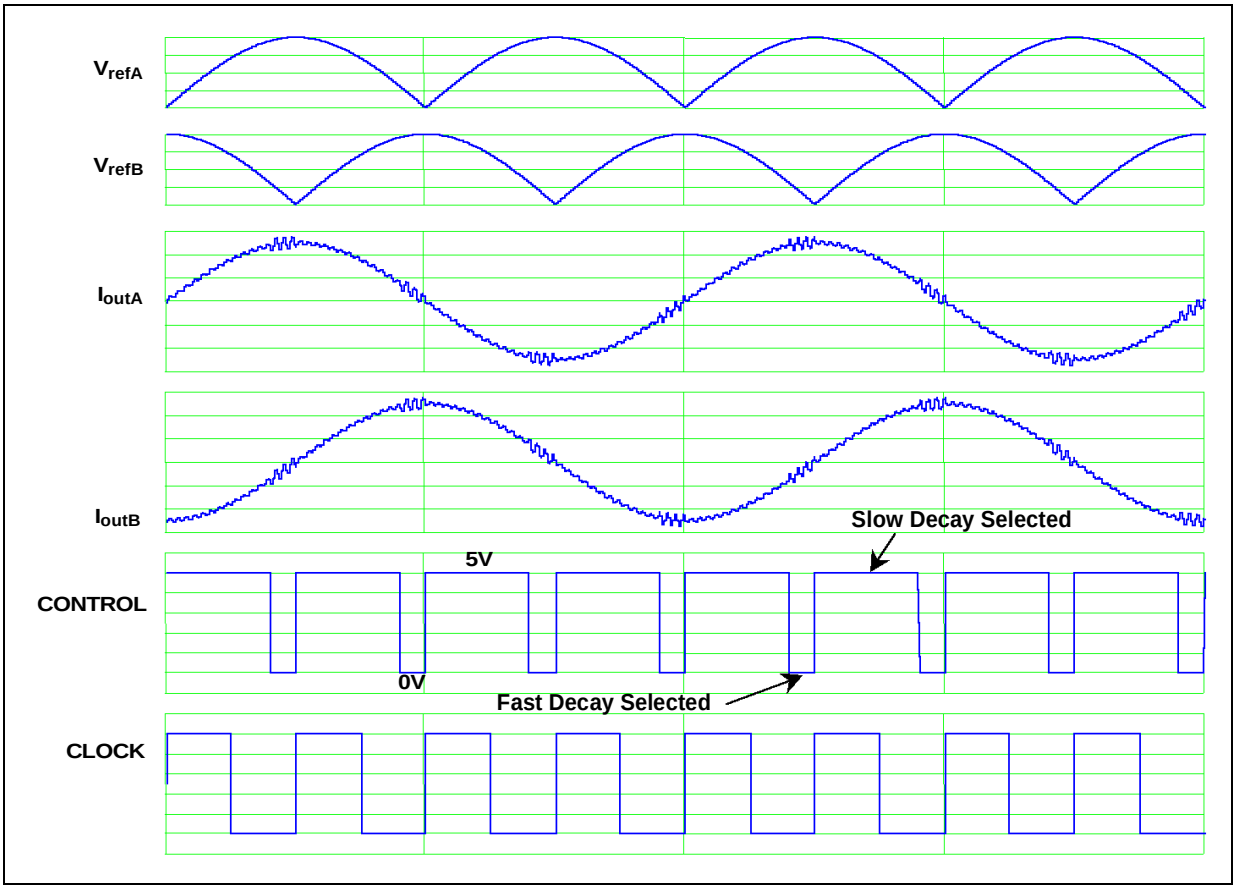


Figure 31. Microstepping reference voltages, output currents and CLOCK signal.



Especially at high rotation speeds, slow decay mode can be inadequate since it does not allow the motor current to decay fast enough, following the decreasing slope of the desired sine wave. In this case it's possible to apply the fast decay mode just during the negative slope of the current (see Figure 32). The disadvantage is an increased current ripple in the other winding (where the current is increasing and fast decay in not needed).

Figure 32. Using Fast decay during high negative current slope.



3 APPLICATION EXAMPLE

Application Data		Motor Data	
Rotation Speed:	300 rpm (f_{CK} = 1kHz)	Winding Resistance:	6.6Ω
Winding peak Current:	1A	Winding Inductance:	7.9mH
Maximum Ripple:	50mA	Step Angle:	1.8°/step
Supply Voltage:	24V ±5%	Maximum BEMF at 300rpm:	15V
Sequence:	Wave Mode		

3.1 Decay mode, sensing resistors and reference voltage.

The first step is choosing the decay type. Let's suppose to implement slow decay, which allows lower power dissipation, lower ripple and avoids voltages below GND at output pins during recirculation. Referring to approximated formulae in Figure 25, it's possible to calculate the Duty-Cycle (D), the Switching Frequency (f_{SW}), the Current Ripple (ΔI). With a 15 µs off-time, we will have:

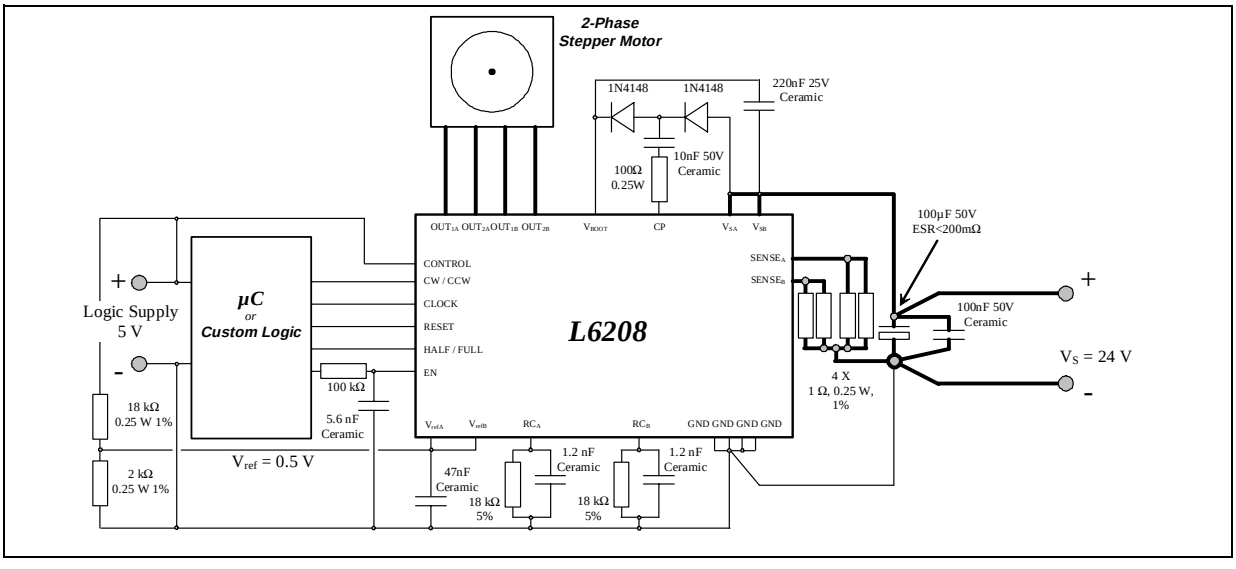
D ≅ 63%, f_{SW} ≅ 25kHz, ΔI ≅ 29mA. The on-time is t_{ON} = D / f_{SW} ≅ 25µs, which is far from the minimum allowed (1.5µs), so slow decay can be used.

The bulk capacitor need to withstand at least 24V + 5% + 25% ≅ 32V. A 50V capacitor will be used. Allowing a voltage ripple of 200mV, the capacitor ESR should be lower than 200mV / 1A = 200mΩ; the AC current capability should be about 1A.

Providing a reference voltage of 0.5V, 0.5Ω sensing resistor are needed. In slow decay mode the resistors power rating is about $P_R \cong I_{rms}^2 \cdot R_{SENSE} \cdot D \cong 0.32W$. Two 1Ω - 0.25W - 1% resistors in parallel are used. The charge pump uses recommended components (1N4148 diodes, ceramic capacitors and a 100Ω resistor to reduce EMI).

R = 18kΩ, C = 1.2 nF are connected to the RC pins, obtaining t_{OFF} ≅ 16µs. On the EN pin a 5.6nF has been placed, and the pin is driven by the µC through a 100kΩ resistor. With these values, in case of short circuit between two OUT pins or an OUT pin and GND, the PowerDMOS turns off after about 1µs, and $t_{DISABLE}$ ≅ 240µs.

Figure 33. Application Example.



With Wave Drive selected, referring to Figure 24, Figure 25, Figure 26, the dissipating power is about 1.36 W. If the ambient temperature is lower than 50°C, with 4cm^2 of copper area on the PCB and a SO24 package, the estimated junction temperature is about 123°C. Using more copper area or a PowerDIP package will reduce the junction temperature.

4 APPENDIX - EVALUATION BOARDS

4.1 PractiSPIN

PractiSPIN is an evaluation and demonstration system that can be used with the PowerSPIN family (L62XX) of devices. A Graphical User Interface (GUI) (see Figure 34) program runs on an IBM-PC under windows and communicates with a common ST7 based interface board (see Figure 35) through the RS232 serial port. The ST7 interface board connects to a device specific evaluation board (target board) via a standard 34 pin ribbon cable interface.

Depending on the target device the PractiSPIN can drive a stepper motor, 1 or 2 DC motors or a brushless DC (BLDC) motor, operating significant parameters such as SPEED, CURRENT, VOLTAGE, DIRECTION, ACCELERATION and DECELERATION RATES from a user friendly graphic interface, and programming a sequence of movements.

The software also allows evaluating the power dissipated by the selected device and, for a given package and dissipating copper area on the PCB, estimates the device's junction temperature.

Figure 34. PractiSPIN PC Software

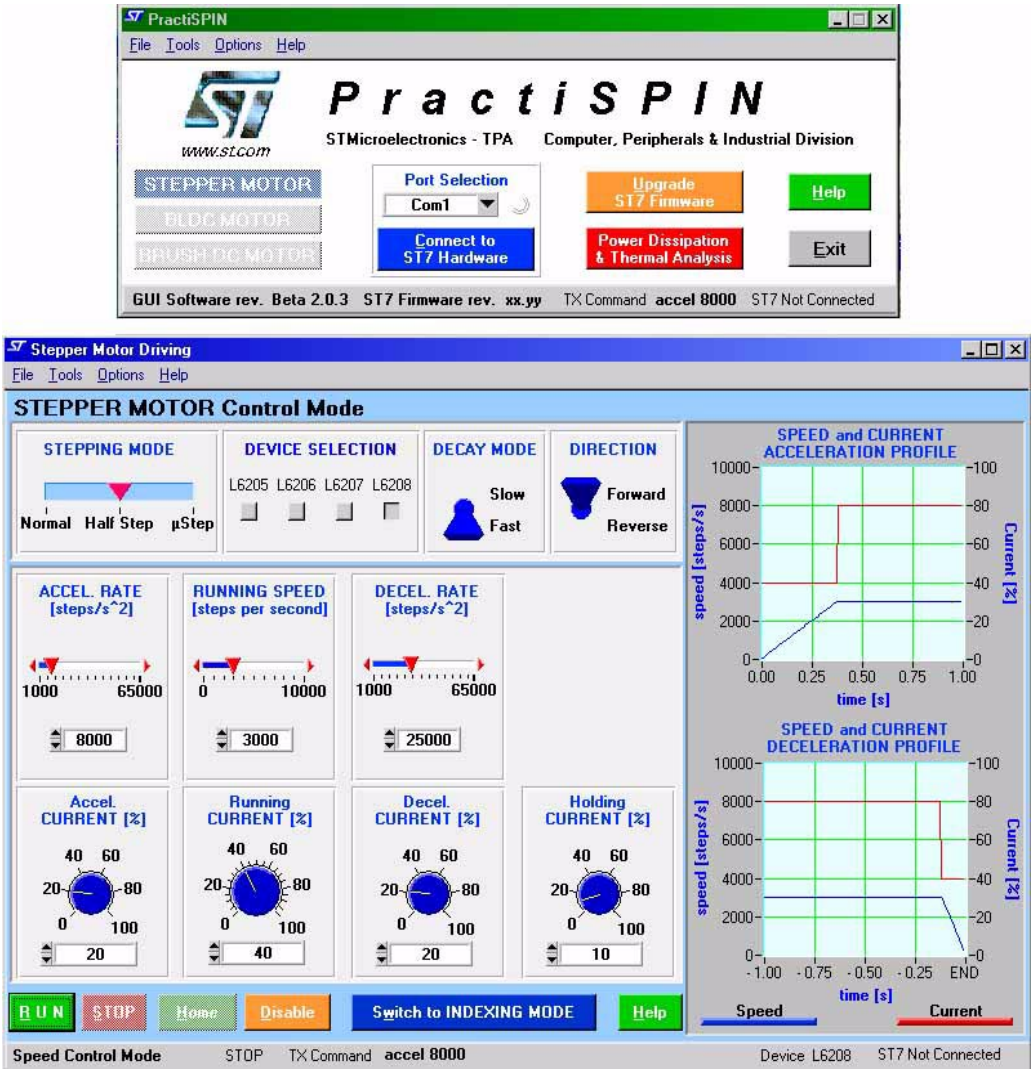


Figure 35. PractiSPIN ST7 Evaluation Board

4.2 EVAL6208N

An evaluation board has been produced to help the evaluation of the device in PowerDIP package. It implements a typical application with several added components. Figure 37 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2, CN3, CN4	2-poles connector	R1	100Ω resistor
CN5	34-poles connector	R2	820Ω 0.6W resistor
C1	220nF/100V Ceramic or Polyester capacitor	R3, R4, R5, R6, R7, R8	10kΩ resistor
C2	220nF/100V Ceramic or Polyester capacitor	R9	4.7kΩ resistor
C3	100µF/63V capacitor	R10, R21	20kΩ 1% resistor
C4	10nF/100V Ceramic capacitor	R11, R12	100kΩ trimmer
C5	10µF/16V Capacitor	R13, R22	2.2kΩ resistor
C6	100nF Capacitor	R14, R15, R16, R17, R18, R19	1Ω 0.4W resistor
C7, C8	68nF Capacitor	R20, R24	5kΩ trimmer
C9, C10	820pF Capacitor	S1	quad switch
D1, D2	1N4148 Diode	U1	L6208N
D3	BZX79C5V1 5.1V Zener Diode	JP1	3-pin jumper

The Evaluation Board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN tool.

The PractiSPIN tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains an upgradeable firmware. This tool allows a fast and easy evaluation of the PowerSPIN family devices, giving the ability of setting the decay mode, the stepping sequence, the output current; to control the motor speed, acceleration and deceleration and to program a sequence of movements.

The PC-software also provides a Power Dissipation and Thermal Analysis section, intended to help a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point designing an application (from the power dissipation and thermal point of view).

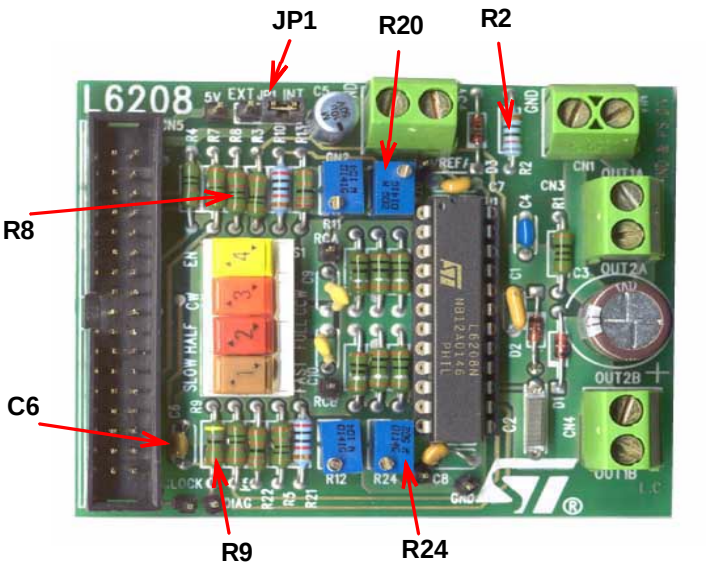
Running the evaluation board in stand-alone mode, instead, four switches (S1) allow enabling the device, setting the direction of the rotation, the type of current decay, the stepping sequence. R20 and R24 set the reference voltage separately for the two bridges, while R13, C7 and R22, C8 are low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Microstepping section). Using external V_{REF} inputs R10, R20, R21, R24 must be disconnected unless the PractiSPIN ST7 evaluation board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN documentation). R11, C9 and R12, C10 are used to set the off-time of the two channels of the IC.

The 5V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R2, D3. Depending on the supply voltage, the value of resistor R2 should be changed in order to ensure a correct biasing of D3.

The jumper JP1 allows choosing the 5V voltage from the internal zener diode network or pin 11 of CN5 (for example an external µC board can provide 5V to the evaluation board). Also CN2 connector can be used to provide an external 5V voltage to the board (in that case R2, D3 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN ST7 board). In this case the current that can be drawn form the board depends on the supply voltage and on R2 value.

Figure 38, Figure 39, Figure 40 show the component placement and the two layers layout of the L6208N Evaluation Board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 36. EVAL6208N.



4.2.1 Important Notes

JP1 : close in INT position for use with PractiSPIN ST7 board

C6 : recommended change to 5.6 nF for safe Overcurrent protection

R8 : recommended change to 100 k for safe Overcurrent protection

R9 : recommended change to 100 k if EN pin is driven from the CN5 connector (for example with PractiSPIN ST7 board) for safe Overcurrent protection

R20, R24 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R2 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D3

4.2.2 Thermal Impedance

EVAL 6208N has been thermally characterized. Figure 41 shows the thermal impedance junction to ambient and the pulsed thermal impedance junction to ambient. This characterization is valid for the device directly soldered into the PCB, without socket.

Figure 37. EVAL6208N Electrical schematic.

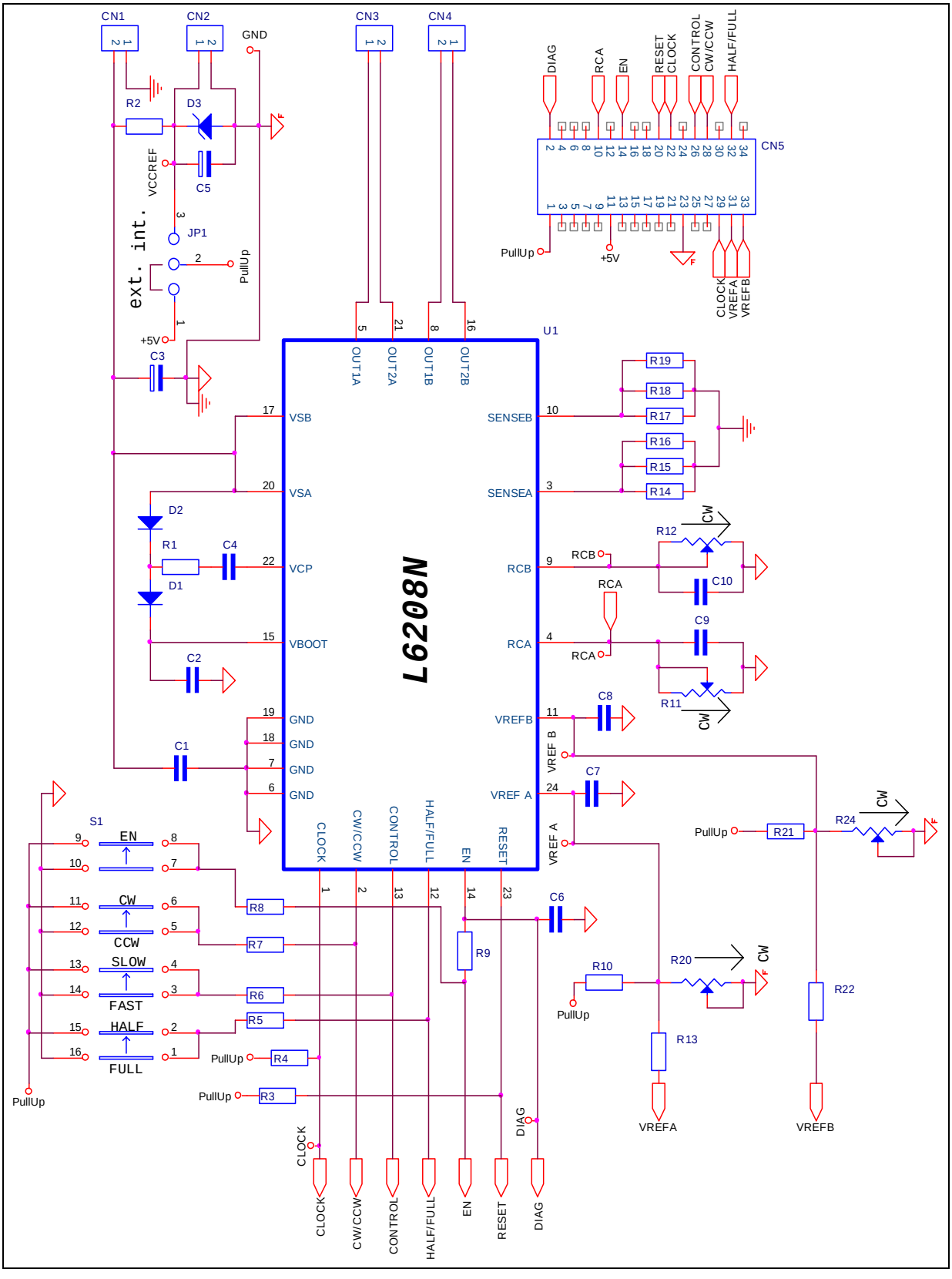


Figure 38. EVAL6208N Component placement.

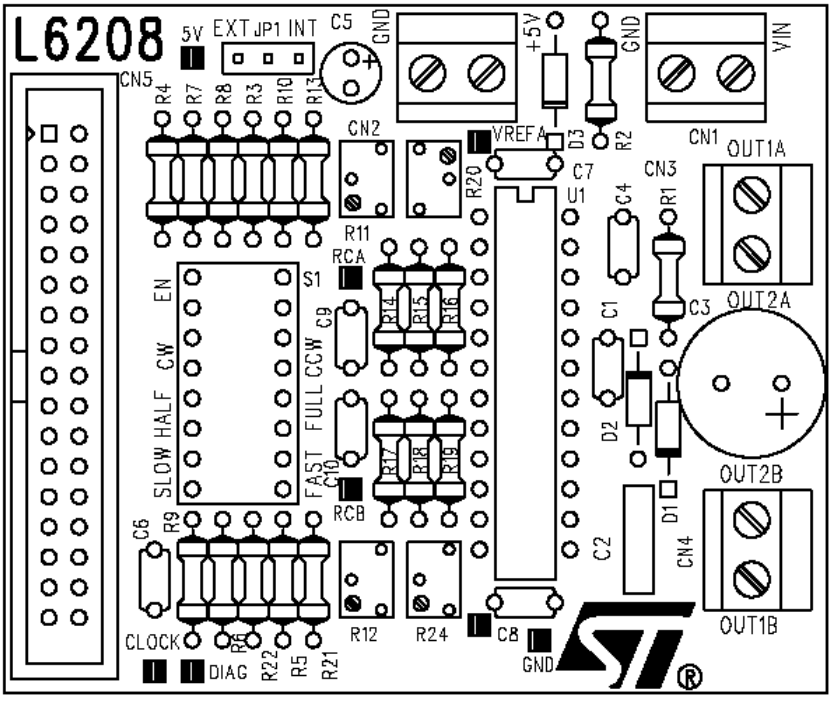


Figure 39. EVAL6208N Top Layer Layout.

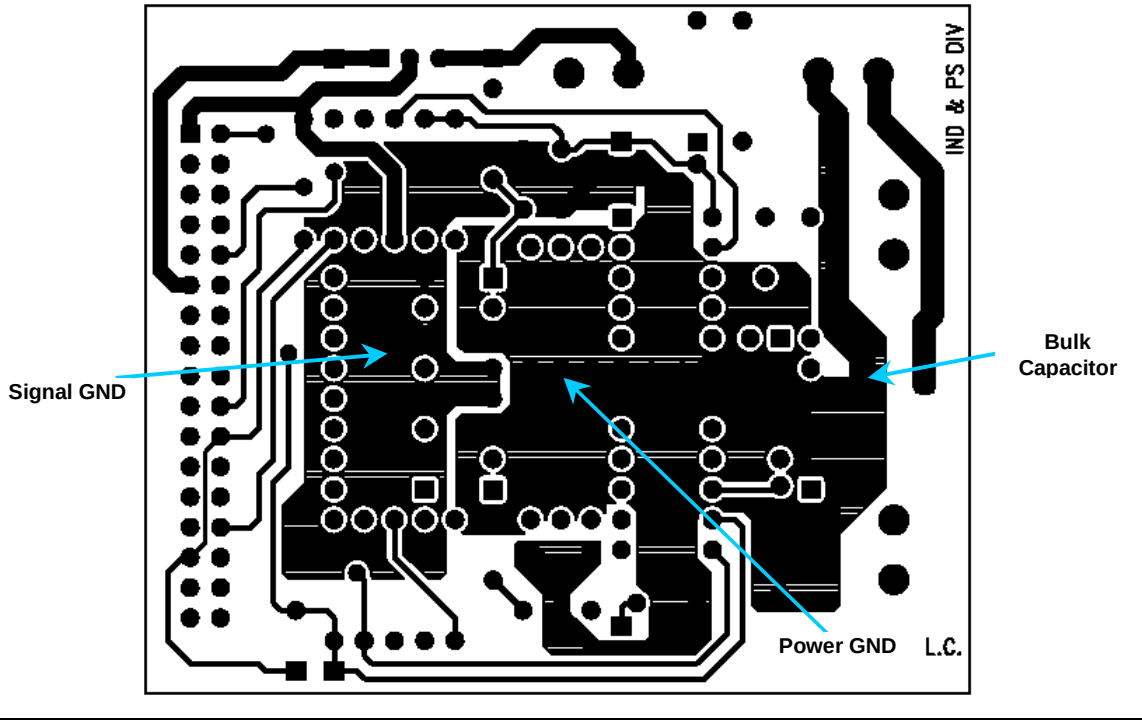


Figure 40. EVAL6208N Bottom Layer Layout.

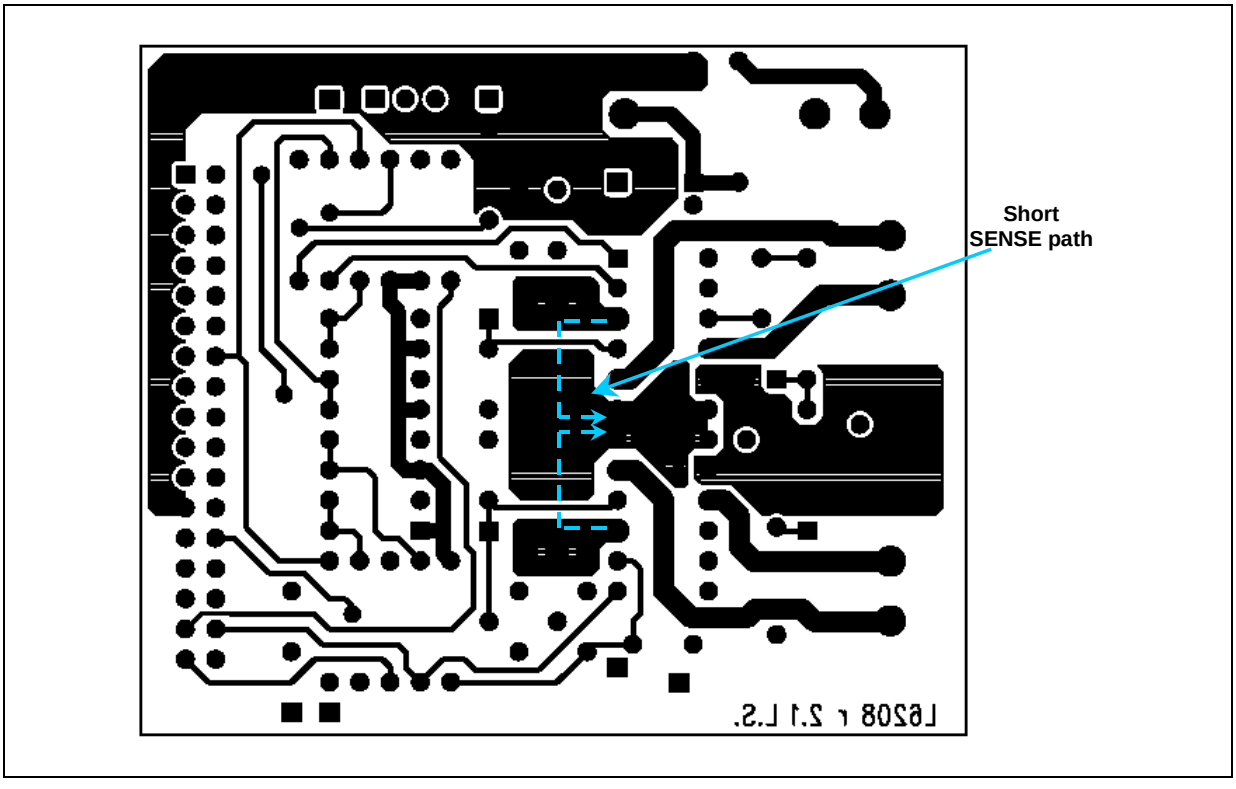
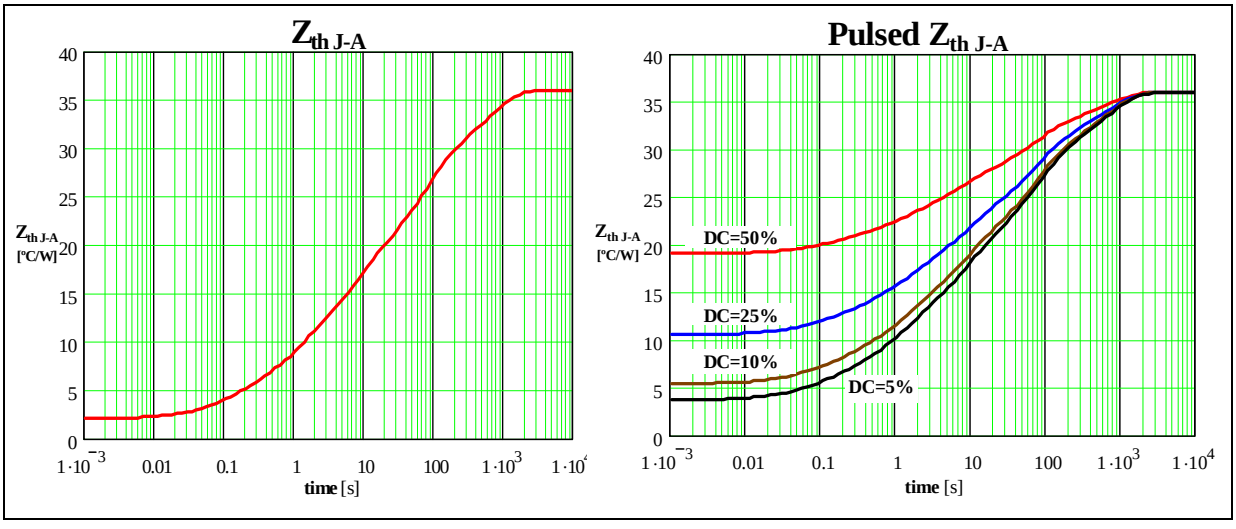


Figure 41. EVAL6208N Thermal impedance Junction to Ambient and pulsed Thermal impedance Junction to Ambient.



4.3 EVAL6208PD

An evaluation board has been produced to help the evaluation of the device in PowerSO package. It implements a typical application with several added components. Figure 43 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2, CN3, CN4	2-poles connector	R1	3.5kΩ 0.6W resistor
CN5	34-poles connector	R2, R3, R4, R5, R6, R7	10kΩ resistor
C1	220nF/100V Ceramic or Polyester capacitor	R3, R4, R5, R6, R7, R8	10kΩ resistor
C2	220nF/100V Ceramic or Polyester capacitor	R8, R17	5kΩ trimmer
C3	100µF/63V capacitor	R9, R19	2.2kΩ resistor
C4	10nF/100V Ceramic capacitor	R10, R11	100kΩ trimmer
C5	10µF/16V Capacitor	R12, R13, R14, R15	0.4Ω 1W resistor
C6, C9	68nF Capacitor	R16, R20	20kΩ 1% resistor
C7, C8	820pF Capacitor	R18	100Ω resistor
C12	100nF Capacitor	R21	4.7kΩ resistor
D1	BAT46SW Diodes	S1	quad switch
D2	BZX79C5V1 5.1V Zener Diode	U1	L6208PD
JP1	3-pin jumper		

The Evaluation Board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN tool.

The PractiSPIN tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains an upgradeable firmware. This tool allows a fast and easy evaluation of the PowerSPIN family devices, giving the ability of setting the decay mode, the stepping sequence, the output current; to control the motor speed, acceleration and deceleration and to program a sequence of movements.

The PC-software also provides a Power Dissipation and Thermal Analysis section, intended to help a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point designing an application (from the power dissipation and thermal point of view).

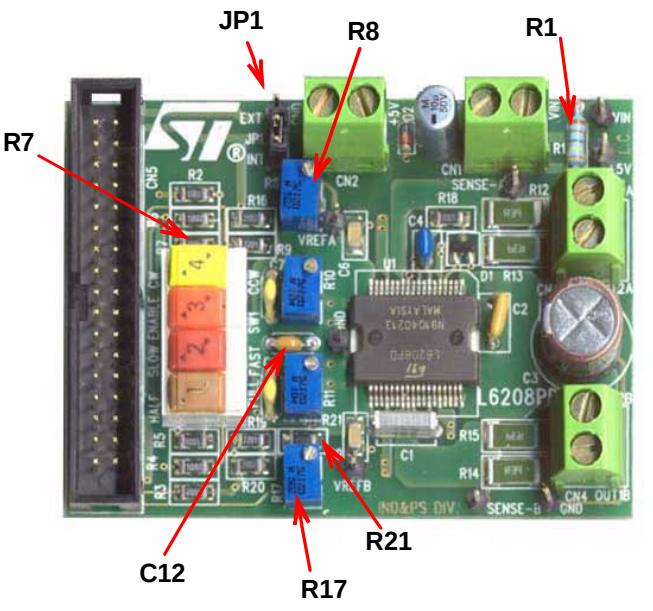
Running the evaluation board in stand-alone mode, instead, four switches (S1) allow enabling the device, setting the direction of the rotation, the type of current decay, the stepping sequence. R8 and R17 set the reference voltage separately for the two bridges, while R9, C6 and R19, C9 are low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Microstepping section). Using external V_{REF} inputs R16, R8, R20, R17 must be disconnected unless the PractiSPIN ST7 evaluation board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN documentation). R10, C7 and R11, C8 are used to set the off-time of the two channels of the IC.

The 5V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R1, D2. Depending on the supply voltage, the value of resistor R1 should be changed in order to ensure a correct biasing of D2.

The jumper JP1 allows choosing the 5V voltage from the internal zener diode network or pin 11 of CN5 (for example an external µC board can provide 5V to the evaluation board). Also CN2 connector can be used to provide an external 5V voltage to the board (in that case R1, D2 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN ST7 board). In this case the current that can be drawn form the board depends on the supply voltage and on R1 value.

Figure 44, Figure 45, Figure 46 show the component placement and the two layers layout of the L6208PD Evaluation Board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 42. EVAL6208PD.



4.3.1 Important Notes

JP1 : close in INT position for use with PractiSPIN ST7 board

C12 : recommended change to 5.6 nF for safe Overcurrent protection

R7 : recommended change to 100 k for safe Overcurrent protection

R21 : recommended change to 100 k if EN pin is driven from the CN5 connector (for example with PractiSPIN ST7 board) for safe Overcurrent protection

R8, R17 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R1 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D2

4.3.2 Thermal Impedance

EVAL 6208PD has been thermally characterized. Figure 47 shows the thermal impedance junction to ambient and the pulsed thermal impedance junction to ambient.

Figure 43. EVAL6208PD Electrical schematic.

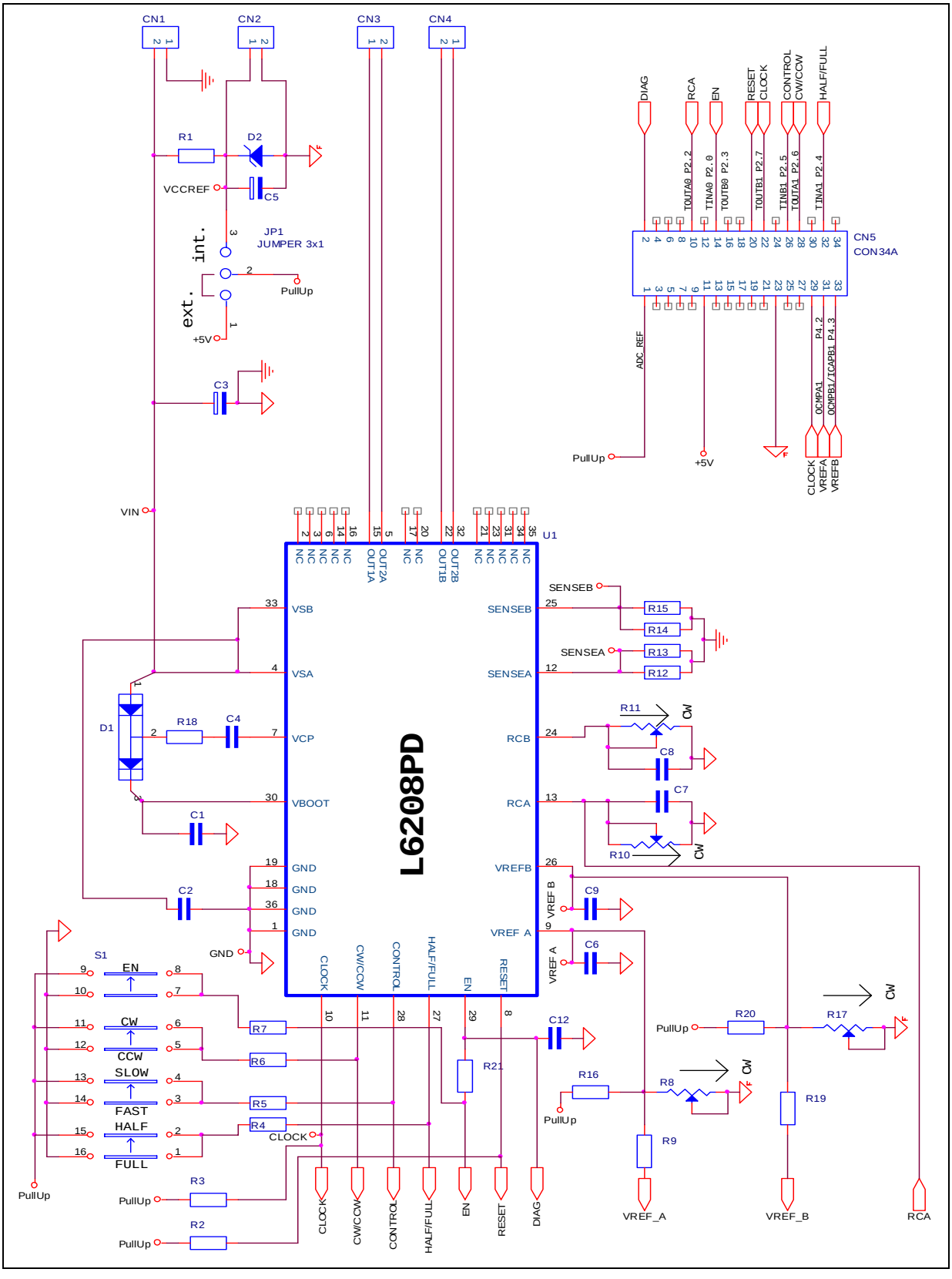


Figure 44. EVAL6208PD Component placement.

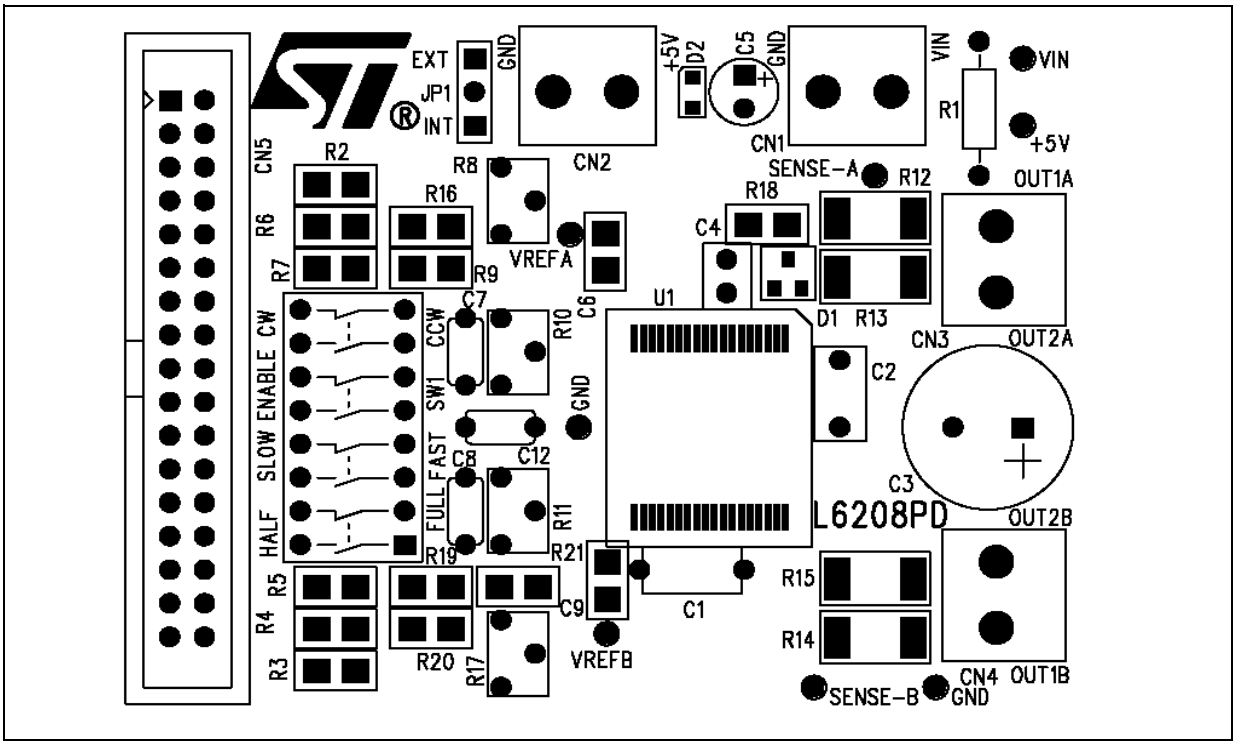


Figure 45. EVAL6208PD Top Layer Layout.

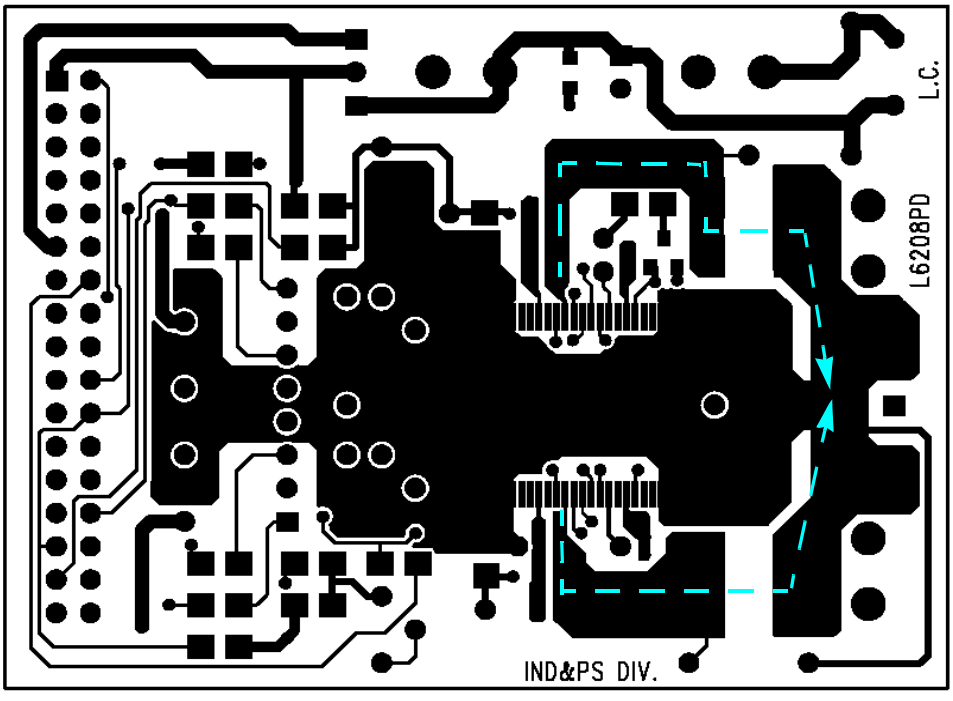


Figure 46. EVAL6208PD Bottom Layer Layout.

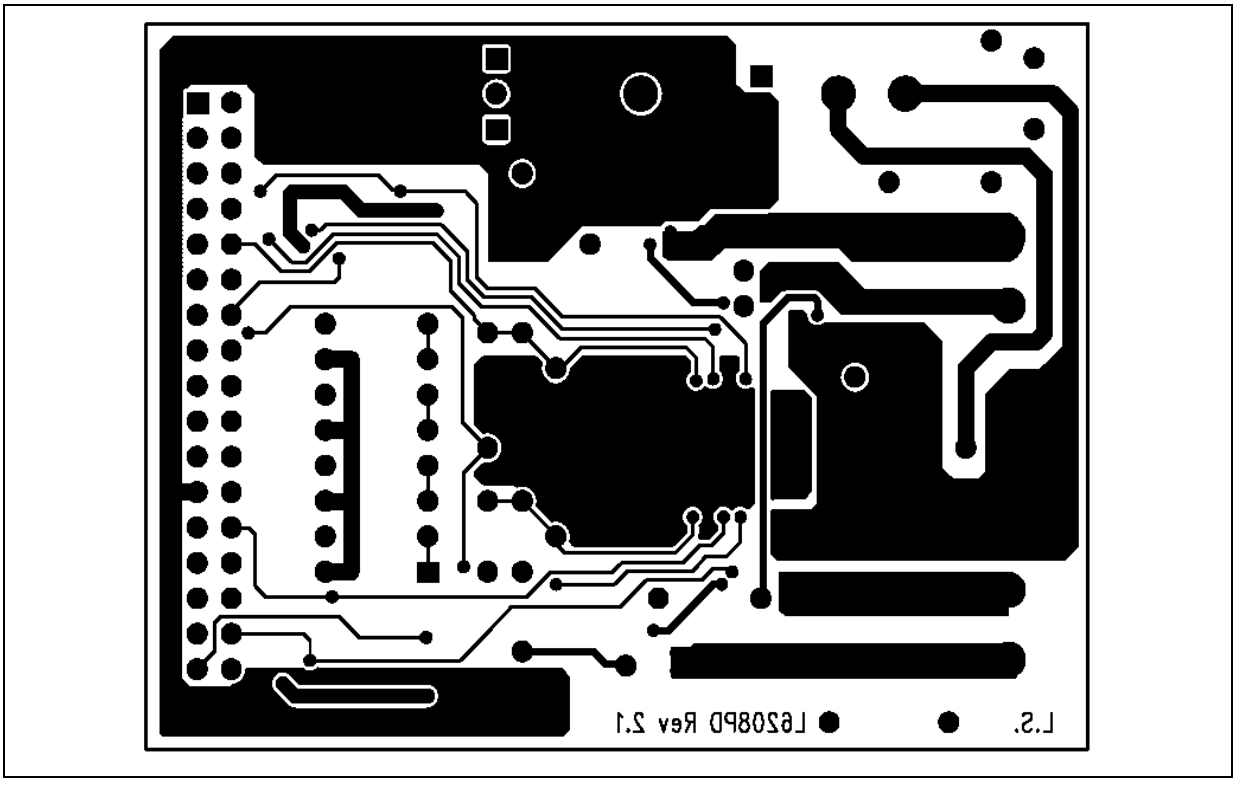
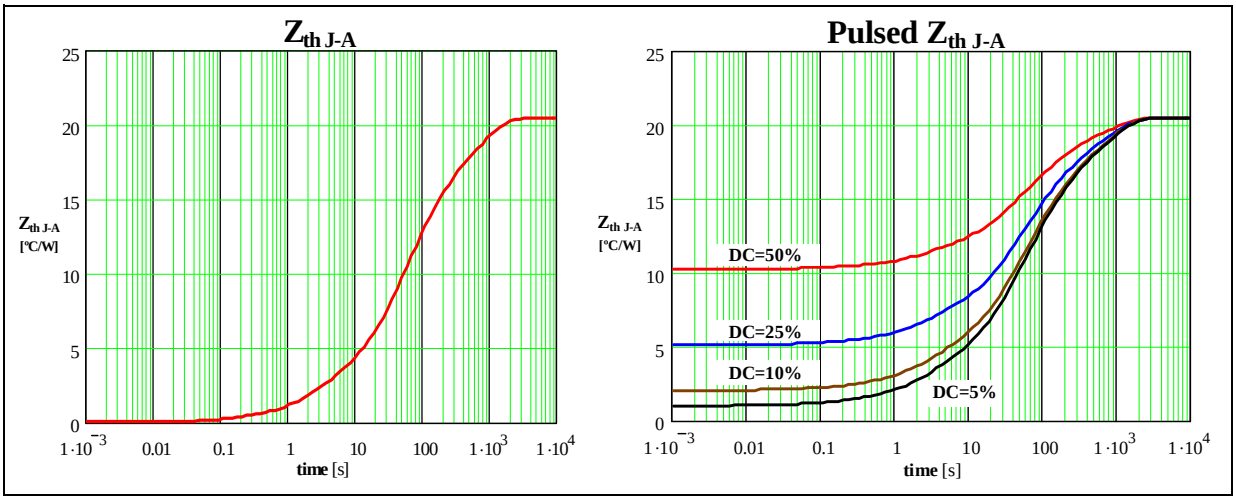


Figure 47. EVAL6208PD Thermal impedance Junction to Ambient and pulsed Thermal impedance Junction to Ambient.



5 REFERENCES

1] D. Arrigo, A. Genova, T. Hopkins, V. Marano, A. Novelli, "A New Fully Integrated Stepper Motor Driver IC", Proceedings of PCIM 2001, September 2001, Intertech Communication.

2] H. Sax, "Stepper Motor Driving" (AN235).

3] T. Hopkins, "Controlling Voltage Transients in Full Bridge Driver Applications" (AN280).

4] T. Hopkins, "Stepper Motor Drive Considerations, Common Problems and Solutions" (AN460).

5] T. Hopkins, K. Kim, "Microstepping Stepper Motor Drive Using Peak Detecting Current Control" (AN1495).

6] P. Casati and C. Cognetti, "A New High Power IC Surface Mount Package Family" (AN668)