To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

M37221M4H/M6H/M8H/MAH–XXXSP/FP
M37221EASP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

1. DESCRIPTION

The M37221M4H/M6H/M8H/MAH-XXXSP/FP are single-chip microcomputers designed with CMOS silicon gate technology. They have a OSD, I^{2}C-BUS interface, and PWM, making them perfect for TV channel selection system.

The M37221EASP/FP have a built-in PROM that can be written electrically.

2. FEATURES

- Number of basic instructions 71
- Memory size
  - ROM .... 16K bytes (M37221M4H-XXXSP/FP)
    24K bytes (M37221M6H-XXXSP/FP)
    32K bytes (M37221M8H-XXXSP/FP)
    40K bytes (M37221MAH-XXXSP/FP, M37221EASP/FP)
  - RAM .... 384 bytes (M37221M4H-XXXSP/FP)
    448 bytes (M37221M6H-XXXSP/FP)
    576 bytes (M37221M8H-XXXSP/FP)
    704 bytes (M37221MAH-XXXSP/FP, M37221EASP/FP)
    (ROM correction memory included)
- The minimum instruction execution time
  .... 0.5 µs (at 8 MHz oscillation frequency)
- Power source voltage .... 5 V ± 10 %
- Subroutine nesting
  maximum 96 levels (M37221M4H/M6H-XXXSP/FP)
  maximum 128 levels (M37221M8H/MAH-XXXSP/FP, M37221EASP/FP)
- Interrupts .... 14 types, 14 vectors
- 8-bit timers 4
- Programmable I/O ports
  (Ports P0, P1, P2, $P3_0$–$P3_2$) 27
- Input ports (Ports $P3_3$, $P3_4$) 2
- Output ports (Ports $P5_2$–$P5_5$) 4
- LED drive ports 4
- Serial I/O .... 8-bit × 1 channel
- Multi-master I^{2}C-BUS interface .... 1 (2 systems)
- A-D comparator (6-bit resolution) .... 6 channels
- D-A converter (6-bit resolution) 2
  Note: Only M37221EASP/FP has D-A converter.

- PWM output circuit ....14-bit × 1, 8-bit × 6
- Power dissipation .... High-speed mode : 165 mW
  (at V_{CC}=5.5V, 8 MHz oscillation frequency, and OSD on)
- ROM correction function .... 2 vectors
- OSD function
  - Display characters .... 24 characters 5 2 lines
    (3 lines or more can be displayed by software)
  - Kinds of characters .... 256 kinds
  - Character display area .... 12 × 16 dots
  - Kinds of character sizes .... 3 kinds
  - Kinds of character colors .... 8 colors (R, G, B)
  - Coloring unit .... character, character background, raster
  - Display position ....
    Horizontal: 64 levels Vertical: 128 levels
  - Attribute .... border

3. APPLICATION

TV

TABLE OF CONTENTS

4. PIN CONFIGURATION

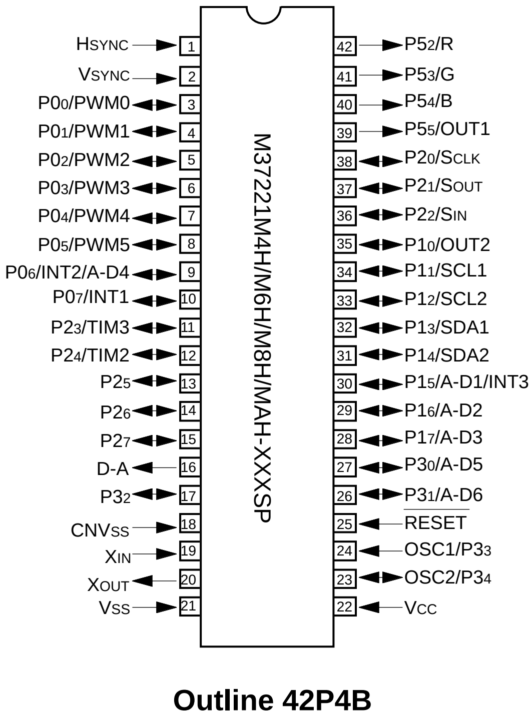


Fig. 4.1 Pin Configuration (1) (Top View)

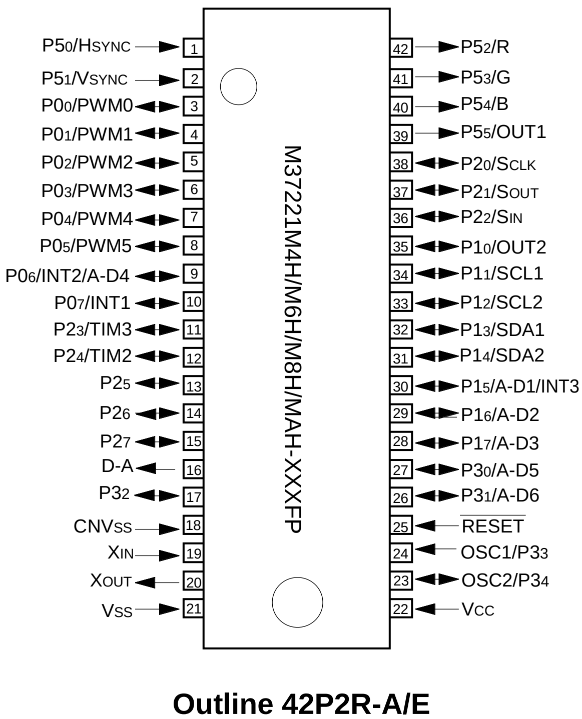
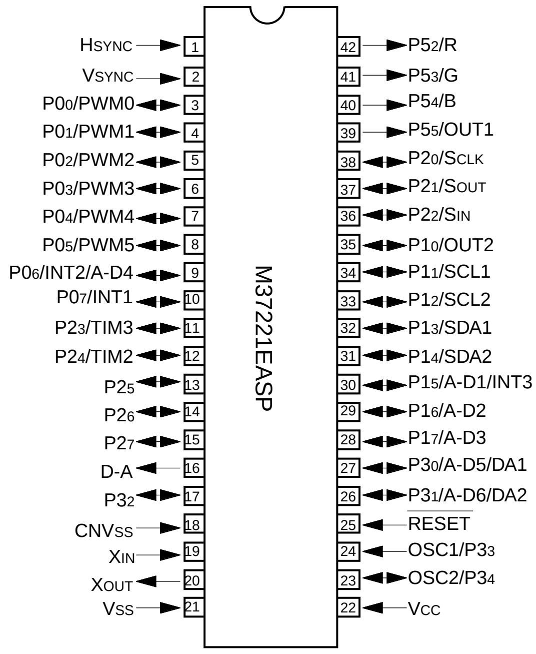
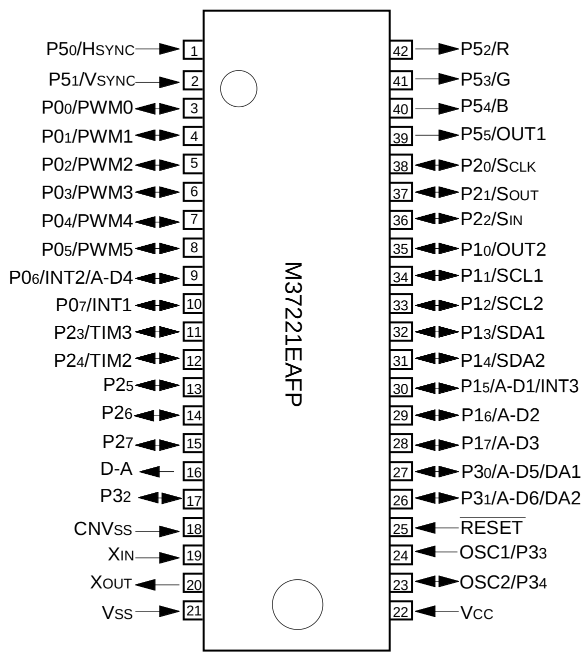


Fig. 4.2 Pin Configuration (2) (Top View)



Outline 42P4B

Fig. 4.3 Pin Configuration (3) (Top View)



Outline 42P2R-A/E

Fig. 4.4 Pin Configuration (4) (Top View)

5. FUNCTIONAL BLOCK DIAGRAM

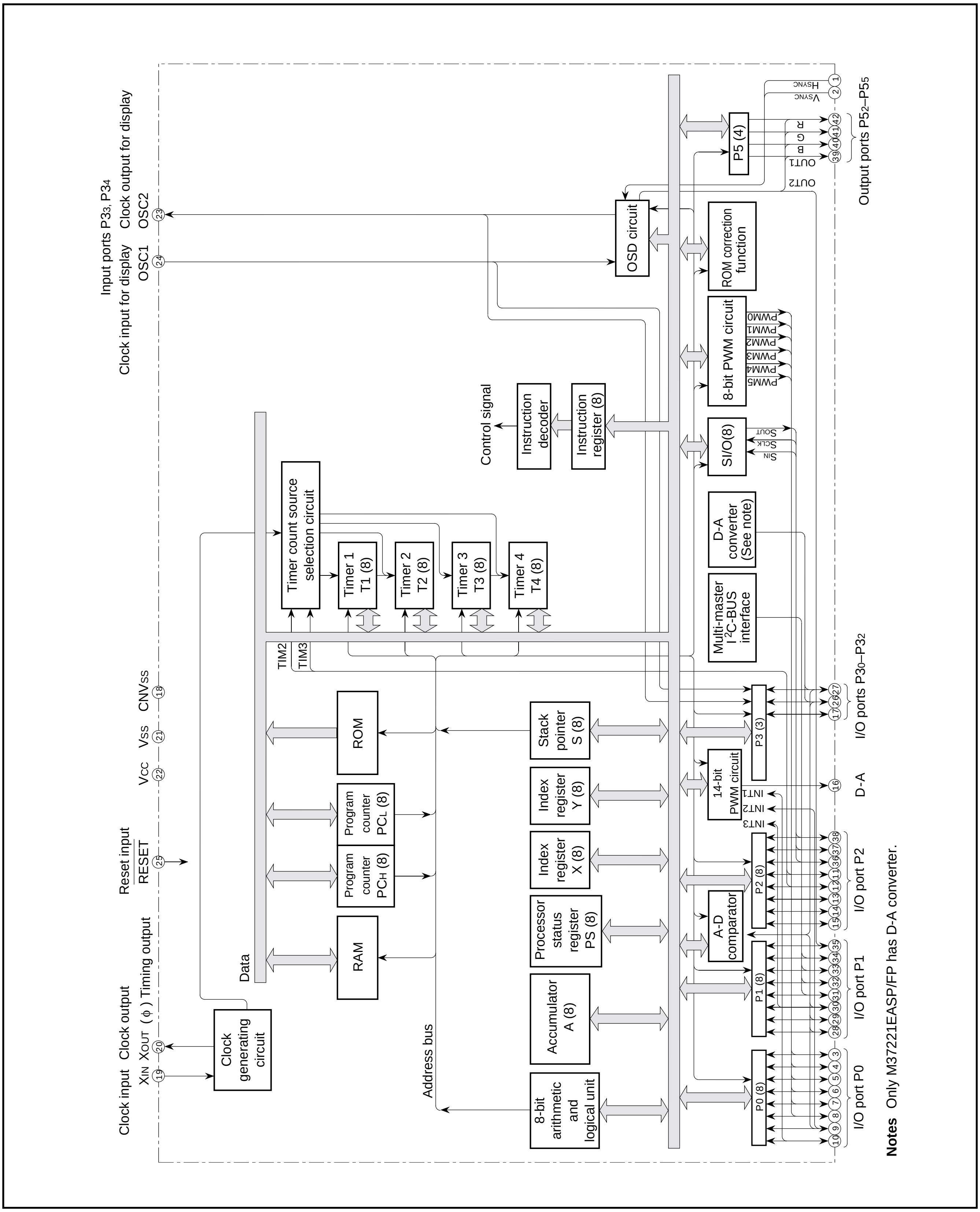


Fig. 5.1 Functional Block Diagram of M37221

6. PERFORMANCE OVERVIEW

Table 6.1 Performance Overview

Parameter			Functions
Number of basic instructions			71
Number of basic instructions			0.5 µs (the minimum instruction execution time, at 8 MHz oscillation fre quency)
Instruction execution time			8 MHz (maximum)
Memory size	ROM	M37221M4H-XXXSP/FP	16K bytes
		M37221M6H-XXXSP/FP	24K bytes
		M37221M8H-XXXSP/FP	32K bytes
		M37221MAH-XXXSP/FP, M37221EASP/FP	40K bytes
	RAM	M37221M4H-XXXSP/FP	384 bytes (ROM correction memory included)
		M37221M6H-XXXSP/FP	448 bytes (ROM correction memory included)
		M37221M8H-XXXSP/FP	576 bytes (ROM correction memory included)
		M37221MAH-XXXSP/FP, M37221EASP/FP	704 bytes (ROM correction memory included)
	OSD ROM		8 K bytes
	OSD RAM		96 bytes
tInput/Output ports	P0	I/O	8-bit 5 1 (N-channel open-drain output structure, can be used as PWM output pins, INT input pins, A-D input pin)
	$P1_0$, $P1_5$–$P1_7$	I/O	4-bit × 1 (CMOS input/output structure, can be used as OSD output pin, A-D input pins, INT input pin)
	$P1_1$–$P1_4$	I/O	4-bit × 1 (CMOS input/output structure, can be used as multi-master I^{2}C-BUS interface)
	$P2_0$, $P2_1$	I/O	2-bit × 1 (CMOS input/output or N-channel open-drain output structure, can be used as serial I/O pins)
	$P2_2$–$P2_7$	I/O	6-bit × 1 (CMOS input/output structure, can be used as serial input pin, timer external clock input pins)
	$P3_0$, $P3_1$	I/O	2-bit × 1 (CMOS input/output or N-channel open-drain output structure, can be used as A-D input pins, D-A conversion output pins <Only M37221EASP/FP>)
	$P3_2$	I/O	1-bit × 1 (N-channel open-drain output structure)
	$P3_3$, $P3_4$	Input	2-bit × 1 (can be used as OSD display clock I/O pins)
	$P5_2$–$P5_5$	Output	4-bit × 1 (CMOS output structure, can be used as OSD output pins)
Serial I/O			8-bit × 1
Multi-master I^{2}C-BUS interface			1 (2 systems)
A-D comparator			6 channels (6-bit resolution)
D-A converter			2 (6-bit resolution) (Only M37221EASP/FP)
PWM output circuit			14-bit × 1, 8-bit × 6
Timers			8-bit timer × 4
ROM correction function			2 vectors
Subroutine nesting	M37221M4H/M6H-XXXSP/FP		96 levels (maximum)
	M37221M8H/MAH-XXXSP/FP, M37221EASP/FP		128 levels (maximum)
Interrupt			<14 sources> INT external interrupt × 3, Internal timer interrupt × 4, Serial I/O interrupt × 1, OSD interrupt × 1, Multi-master I^{2}C-BUS interface interrupt × 1, $f(X_{IN})/4096$ interrupt × 1, V_{SYNC} interrupt × 1, BRK interrupt × 1, Reset × 1
Clock generating circuit			2 built-in circuits (externally connected a ceramic resonator or a quartz-crystal oscillator)

Table 6.2 Performance Overview (continued)

Parameter			Functions
OSD display function	Number of display characters		24 characters × 2 lines
	Dot structure		12 × 16 dots
	Kinds of characters		256 kinds
	Kinds of character sizes		3 kinds
	Character font coloring		1 screen: 8 kinds (per character unit)
	Display position		Horizontal: 64 levels, Vertical: 128 levels
Power source voltage			5 V ± 10 %
Power dissipation		OSD ON	165 mW typ. (at oscillation frequency f(X_{IN}) = 8 MHz, f_{OSC} = 8 MHz)
		OSD OFF	110 mW typ. (at oscillation frequency f(X_{IN}) = 8 MHz)
		In stop mode	1.65 mW (maximum)
Operating temperature range			–10 °C to 70 °C
Device structure			CMOS silicon gate process
Package	M37221M4H/M6H/M8H/MAH-XXXSP, M37221EASP		42-pin plastic molded SDIP
	M37221M4H/M6H/M8H/MAH-XXXFP, M37221EAFP		42-pin plastic molded SSOP

7. PIN DESCRIPTION

Table 7.1 Pin Description

Pin	Name	Input/ Output	Name
V_{CC}, V_{SS}.	Power source		Apply voltage of 5 V ± 10 % (typical) to V_{CC}, and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a “L” for 2 μs or more (under normal V_{CC} conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this “L” condition should be maintained for the required time.
X_{IN}	Clock input	Input	This is the input pin for the main clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins X_{IN} and X_{OUT}. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$P0_0$/PWM0–$P0_5$/PWM5, $P0_6$/INT2/ A-D4, $P0_7$/INT1	I/O port P0	I/O	Port P0 is an 8-bit I/O port with a direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open-drain output (See note 1.)
	PWM output	Output	Output Pins $P0_0$ to $P0_5$ are also used as PWM output pins PWM0 to PWM4, respectively. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pins $P0_6$, $P0_7$ are also used as external interrupt input pins INT2 and INT1 respectively.
	Analog input	Input	$P0_6$ pin is also used as analog input pin A-D4.
$P1_0$/OUT2, $P1_1$/SCL1, $P1_2$/SCL2, $P1_3$/SDA1, $P1_4$/SDA2, $P1_5$/A-D1/ INT3, $P1_6$/A-D2, $P1_7$/A-D3	I/O port P1	I/O	I/O Port P1 is a 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output (See note 1.)
	OSD output	Output	Pins $P1_0$ is also used as OSD output pin OUT2. The output structure is CMOS output.
	Multi-master I^2C-BUS interface	I/O	Pins $P1_1$–$P1_4$ are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I^2C-BUS interface is used. The output structure is N-channel open-drain output.
	Analog input	Input	Pins $P1_5$–$P1_7$ are also used as analog input pins A-D1 to A-D3 respectively.
	External interrupt input	Input	$P1_5$ pin is also used as external interrupt input pin INT3.
$P2_0$/S_{CLK}, $P2_1$/S_{OUT}, $P2_2$/S_{IN}, $P2_3$/TIM3, $P2_4$/TIM2, $P2_5$–$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output. The output structure is CMOS output (See note 1.)
	Timer external clock input	Input	Pins $P2_3$, $P2_4$ are also used as timer external clock input pins TIM3, TIM2 respectively.
	Serial I/O synchro-nizing clock input/ output	I/O	$P2_0$ pin is also used as serial I/O synchronizing clock input/output pin S_{CLK}. The output structure is N-channel open-drain output.
	Serial I/O data input/output	I/O	Pins $P2_1$, $P2_2$ are also used as serial I/O data input/output pins S_{OUT}, S_{IN} respectively. The output structure is N-channel open-drain output.
$P3_0$/A-D5/ DA1, $P3_1$/A-D6/ DA2, $P3_2$	I/O port P3	I/O	Ports $P3_0$–$P3_2$ are a 3-bit I/O port and has basically the same functions as port P0. Either CMOS output or N-channel open-drain output structure can be selected as the port $P3_0$ and $P3_1$. The output structure of port $P3_2$ is N-channel open-drain output. (See notes 1, 2)
	Analog input	Input	Pins $P3_0$, $P3_1$ are also used as analog input pins A-D5, A-D6 respectively.
	D-A conversion output	Output	Pins $P3_0$, $P3_1$ are also used as D-A conversion output pins DA1, DA2 respectively. (See note 3)
$P3_3$/OSC1, $P3_4$/OSC2	Input port P3	Input	Ports $P3_3$, $P3_4$ are a 2-bit input port.
	Clock input for OSD	Input	$P3_3$ pin is also used as OSD clock input pin OSC1.
	Clock output for OSD	Output	$P3_4$ pin is also used as OSD clock output pin OSC2. The output structure is CMOS output.

Table 7.2 Pin Description (continued)

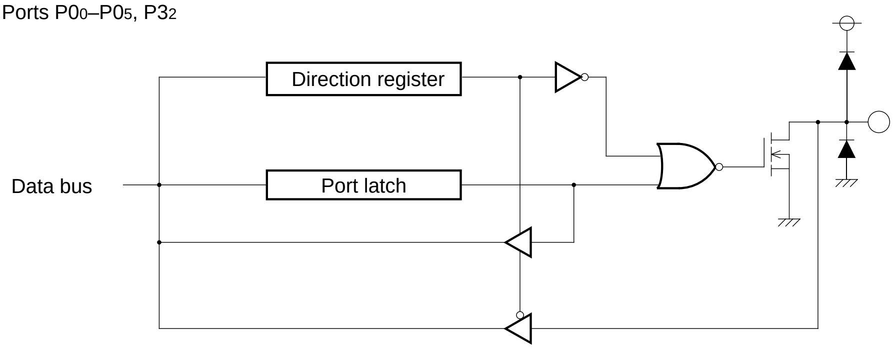
$P5_2$/R, $P5_3$/G, $P5_4$/B, $P5_5$/OUT1	Output port P5	Output	Ports $P5_2$–$P5_5$ are a 4-bit output port. The output structure is CMOS output.
	OSD output	Output	Pins $P5_2$–$P5_5$ are also used as OSD output pins R, G, B, OUT1 respectively. The output structure is CMOS output.
H_{SYNC}	H_{SYNC} input	Input	This is a horizontal synchronizing signal input for OSD.
V_{SYNC}	V_{SYNC} input	Input	This is a vertical synchronizing signal input for OSD.
D-A	DA output	Output	This is a 14-bit PWM output pin.

Note 1 : Port Pi (i = 0 to 3) has a port Pi direction register that can be used to program each bit for input (“0”) or an output (“1”). The pins programmed as “1” in the direction register are output pins. When pins are programmed as “0,” they are input pins. When pins are programmed as output pins, the output data is written into the port latch and then output. When data is read from the output pins, the data of the port latch, not the output pin level, is read. This allows a previously output value to be read correctly even if the output LOW voltage has risen due to, for example, a directly-driven light emitting diode. The input pins are in the floating state, so the values of the pins can be read. When data is written to the input pin, it is written only into the port latch, while the pin remains in the floating state.

2 : To swich output structures, set by the following bits.
$P3_0$: bit 0 of port P3 output mode control register
$P3_1$: bit 1 of port P3 output mode control register
When “0,” CMOS output; when “1,” N-channel open-drain output.

3: Only M37221EASP/FP have a built-in D-A converter.

Ports P0$_0$–P0$_5$, P3$_2$

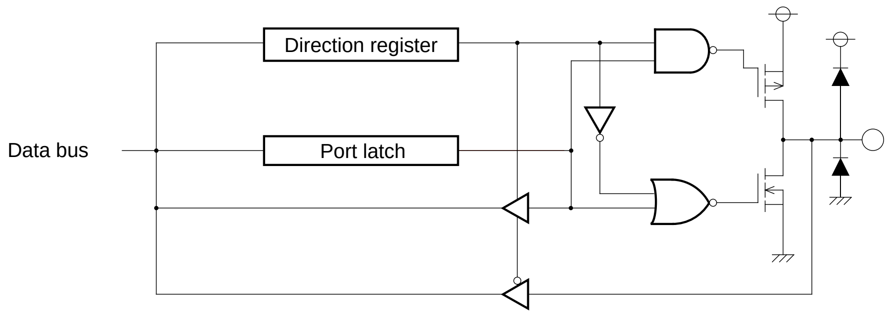


N-channel open drain output

Ports P0$_0$–P0$_5$, P3$_2$

Note: Each port is also used as follows:
P0$_0$–P0$_5$: PWM0–PWM5

Ports P1, P2, P3$_0$, P3$_1$



CMOS output

Ports P1, P2, P3$_0$, P3$_1$

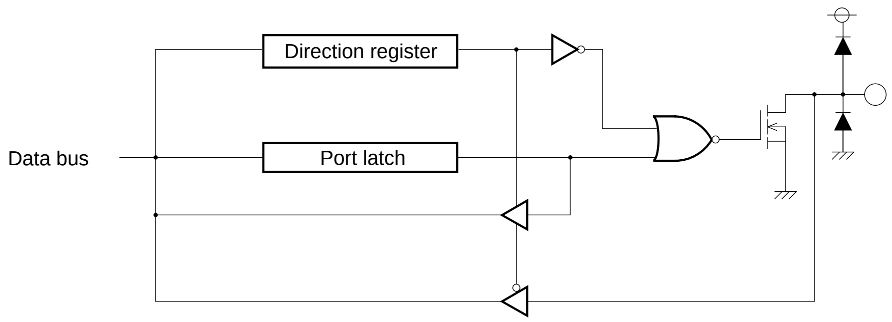
Notes 1: Each port is also used as follows:

P1$_0$: OUT2	P2$_0$: SCLK
P1$_1$: SCL1	P2$_1$: SOUT
P1$_2$: SCL2	P2$_2$: SIN
P1$_3$: SDA1	P2$_3$: TIM3
P1$_4$: SDA2	P2$_4$: TIM2
P1$_5$: A-D1/INT3	P3$_0$: A-D5/DA1
P1$_6$: A-D2	P3$_1$: A-D6/DA2
P1$_7$: A-D3	

2: The output structure of ports P1$_1$–P1$_4$ is N-channel open-drain output when using as multi-master I^{2}C-BUS inter face (it is the same with ports P0$_6$ and P0$_7$)

3: The output structure of ports P3$_0$ and P3$_1$ can be selected either CMOS output or N-channel open-drain output (it is the same with ports P0$_6$ and P0$_7$)

Ports P0$_6$, P0$_7$



N-channel open-drain output

Ports P0$_6$, P0$_7$

Note: Each port is also used as follow:
P0$_6$: INT2/A-D4
P0$_7$: INT1

Fig. 7.1 I/O pin block diagram (1)

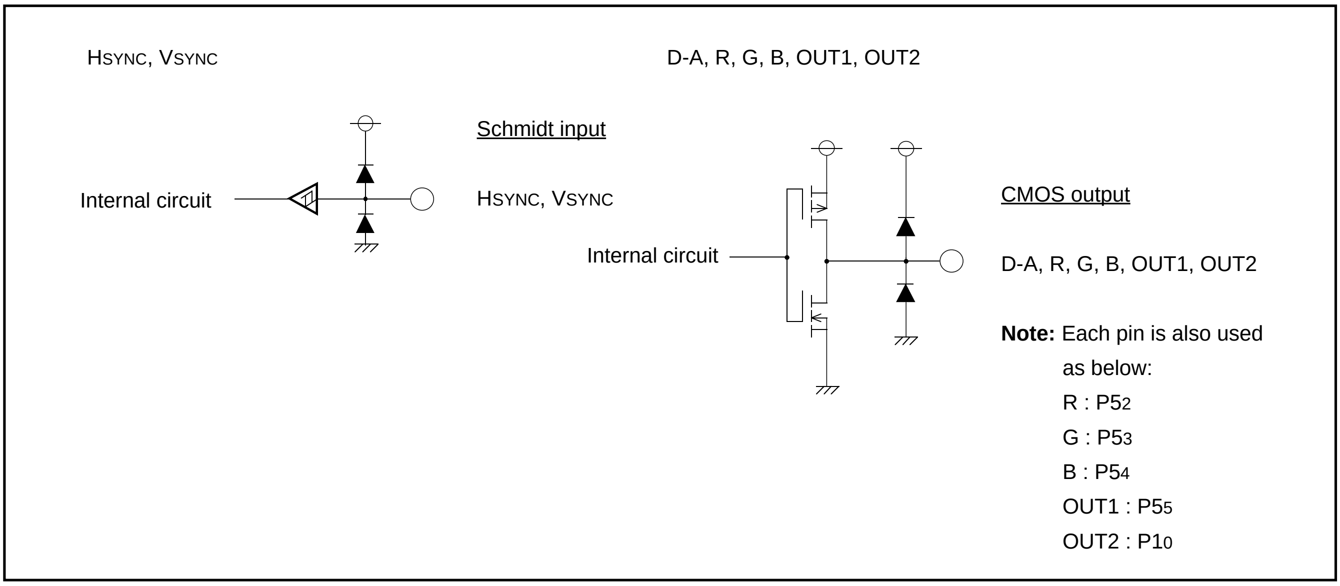


Fig. 7.2 I/O pin block diagram (2)

8. FUNCTION BLOCK DESCRIPTION
8.1 CENTRAL PROCESSING UNIT (CPU)

This microcomputer uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.
Availability of 740 Family instructions is as follows:
The FST and SLW instructions cannot be used.
The MUL, DIV, WIT and STP instructions can be used.

8.1.1 CPU Mode Register

The CPU mode register includes a stack page selection bit and internal system clock selection bit. The CPU mode register is allocated to address $00FB_{16}$.

CPU Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1		0	0

CPU mode register (CM) [Address $00FB_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Fix these bits to "0."		Indeterminate	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3 to 7	Fix these bits to "1."		Indeterminate	R	W

Note: This bit is set to "1" after the reset release.

Fig. 8.1.1 CPU Mode Register

8.2 MEMORY
8.2.1 Special Function Register (SFR) Area
The special function register (SFR) area in the zero page includes control registers such as I/O ports and timers.

8.2.2 RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

8.2.3 ROM
ROM is used for storing user programs as well as the interrupt vector area.

8.2.4 OSD RAM
RAM used for specifying the character codes and colors for display.

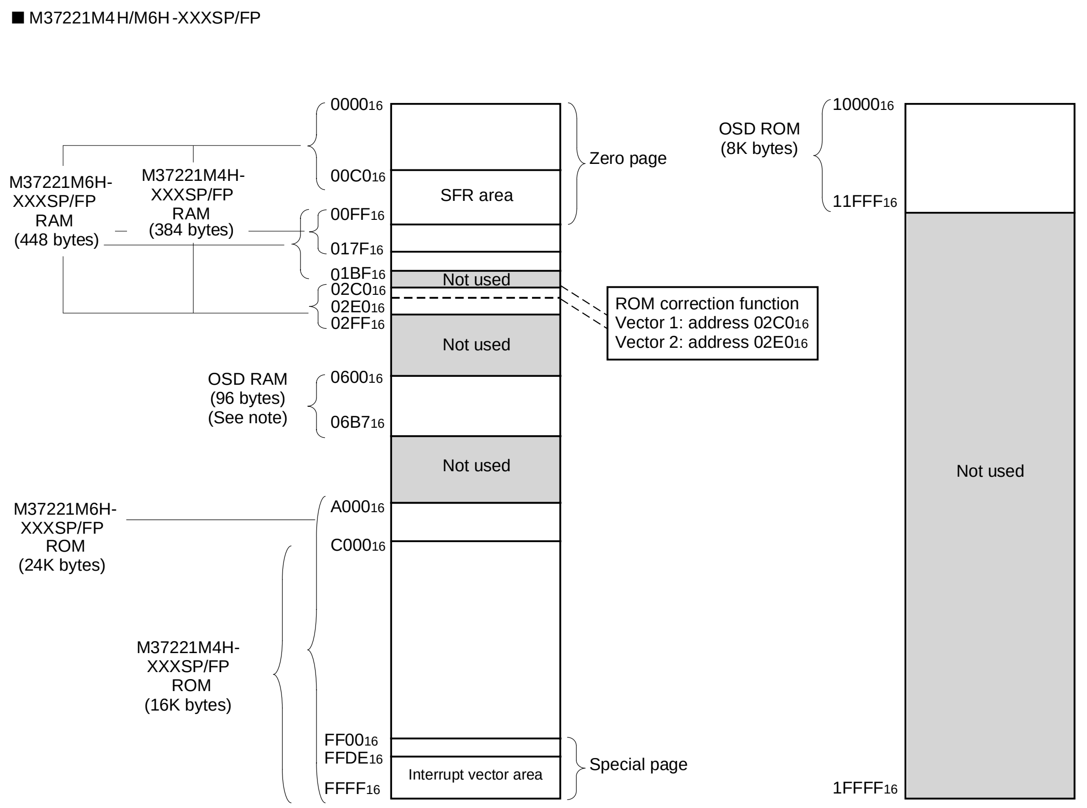
8.2.5 OSD ROM
ROM used for storing character data for display.

8.2.6 Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

8.2.7 Zero Page
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area is possible with only 2 bytes in the zero page addressing mode.

8.2.8 Special Page
The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area is possible with only 2 bytes in the special page addressing mode.

8.2.9 ROM Correction Memory (RAM)
This is used as the program area for ROM correction.



Note: Refer to Table 8.11.4 OSD RAM.

Fig. 8.2.1 Memory Map (M37221M4H/M6H-XXXSP/FP)

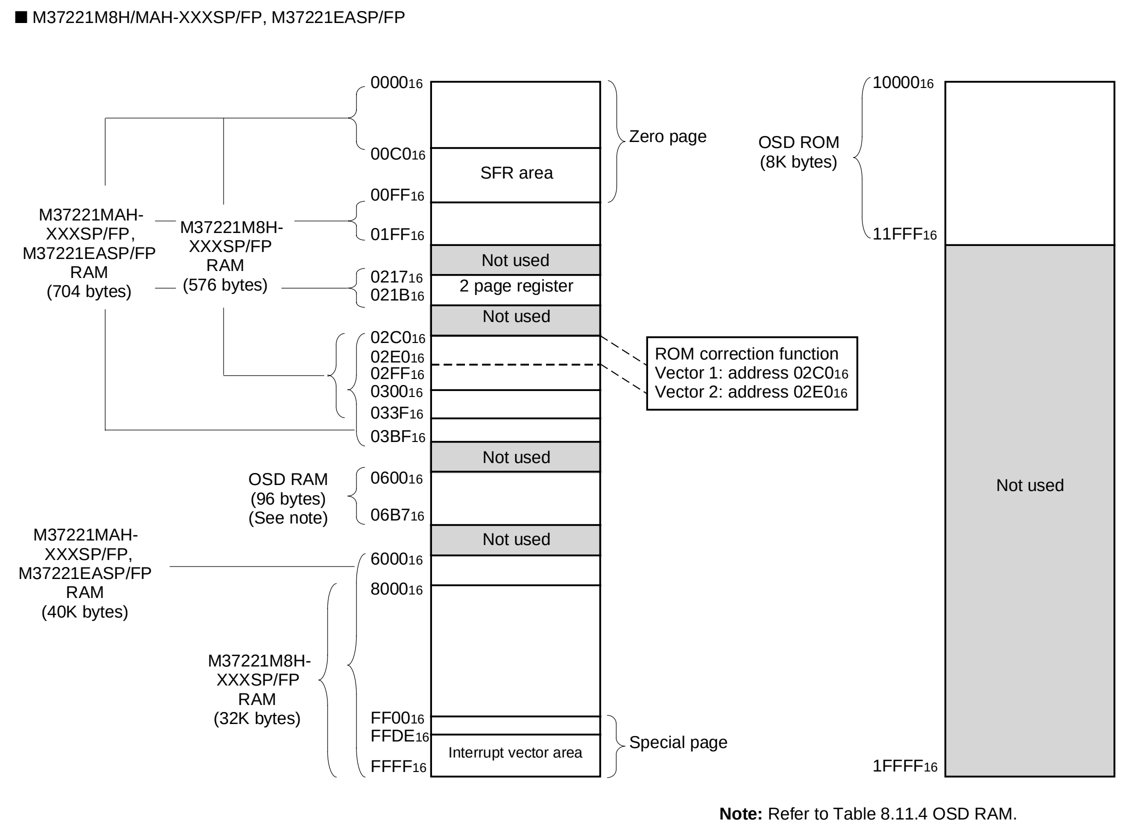


Fig. 8.2.2 Memory Map (M37221M8H/MAH-XXXSP/FP, M37221EASP/FP)

■ SFR area (addresses C0$_{16}$ to DF$_{16}$)

<Bit allocation>

- [ ] : / [Name] : } Function bit
- (shaded) : No function bit
- [0] : Fix to this bit to "0" (do not write to "1")
- [1] : Fix to this bit to "1" (do not write to "0")

State immediately after reset>

- [0] : "0" immediately after reset
- [1] : "1" immediately after reset
- [?] : Indeterminate immediately after reset

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7 … b0)
C0$_{16}$	Port P0 (P0)									?
C1$_{16}$	Port P0 direction register (D0)									00$_{16}$
C2$_{16}$	Port P1 (P1)									?
C3$_{16}$	Port P1 direction register (D1)									00$_{16}$
C4$_{16}$	Port P2 (P2)									?
C5$_{16}$	Port P2 direction register (D2)									00$_{16}$
C6$_{16}$	Port P3 (P3)									0 0 0 ? ? ? ? ?
C7$_{16}$	Port P3 direction register (D3)									00$_{16}$
C8$_{16}$										?
C9$_{16}$										?
CA$_{16}$	Port P5 (P5)									0 0 ? ? ? ? ? ?
CB$_{16}$	Port P5 direction register (D5)									00$_{16}$
CC$_{16}$										?
CD$_{16}$	Port P3 output mode control register (P3S) (Note 1)					DA2S	DA1S	P31S	P30S	00$_{16}$
CE$_{16}$	DA-H register (DA-H)									?
CF$_{16}$	DA-L register (DA-L)									0 0 ? ? ? ? ? ?
D0$_{16}$	PWM0 register (PWM0)									?
D1$_{16}$	PWM1 register (PWM1)									?
D2$_{16}$	PWM2 register (PWM2)									?
D3$_{16}$	PWM3 register (PWM3)									?
D4$_{16}$	PWM4 register (PWM4)									?
D5$_{16}$	PWM output control register 1 (PW)	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00$_{16}$
D6$_{16}$	PWM output control register 2 (PN)				PN4	PN3	PN2			00$_{16}$
D7$_{16}$	I^{2}C data shift register (S0)									?
D8$_{16}$	I^{2}C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00$_{16}$
D9$_{16}$	I^{2}C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0 0 0 1 0 0 0 ?
DA$_{16}$	I^{2}C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ES0	BC2	BC1	BC0	00$_{16}$
DB$_{16}$	I^{2}C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00$_{16}$
DC$_{16}$	Serial I/O mode register (SM)		SM6	SM5	0	SM3	SM2	SM1	SM0	00$_{16}$
DD$_{16}$	Serial I/O regsiter (SIO)									?
DE$_{16}$	DA1 conversion register (DA1) (Note 2)		0	DA15	DA14	DA13	DA12	DA11	DA10	0 0 ? ? ? ? ? ?
DF$_{16}$	DA2 conversion register (DA2) (Note 2)		0	DA25	DA24	DA23	DA22	DA21	DA20	0 0 ? ? ? ? ? ?

Note 1: As for M37221M4H/M6H/M8H/MAH-XXXSP/FP, fix bits 2 and 3 to "0."
2: M37221M4H/M6H/M8H/MAH-XXXSP/FP do not have this register. Fix this register to "00$_{16}$."

Fig. 8.2.3 Memory Map of Special Function Register (SFR) (1)

■ SFR area (addresses $E0_{16}$ to FF_{16})

<Bit allocation>

- (blank box) : Function bit
- Name : Function bit
- (shaded box) : No function bit
- 0 : Fix to this bit to “0” (do not write to “1”)
- 1 : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- 0 : “0” immediately after reset
- 1 : “1” immediately after reset
- ?

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7 … b0)
$E0_{16}$	Horizontal register (HR)			HR5	HR4	HR3	HR2	HR1	HR0	00_{16}
$E1_{16}$	Vertical register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0 ? ? ? ? ? ? ?
$E2_{16}$	Vertical register 2 (CV2)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0 ? ? ? ? ? ? ?
$E3_{16}$										?
$E4_{16}$	Character size register (CS)					CS21	CS20	CS11	CS10	0 0 0 0 ? ? ? ?
$E5_{16}$	Border selection register (MD)						MD20		MD10	0 0 0 0 0 ? 0 ?
$E6_{16}$	Color register 0 (CO0)	CO07	CO06	CO05	CO04	CO03	CO02	CO01		00_{16}
$E7_{16}$	Color register 1 (CO1)	CO17	CO16	CO15	CO14	CO13	CO12	CO11		00_{16}
$E8_{16}$	Color register 2 (CO2)	CO27	CO26	CO25	CO24	CO23	CO22	CO21		00_{16}
$E9_{16}$	Color register 3 (CO3)	CO37	CO36	CO35	CO34	CO33	CO32	CO31		00_{16}
EA_{16}	OSD control register (CC)	CC7					CC2	CC1	CC0	00_{16}
EB_{16}										?
EC_{16}	OSD port control register (CRTP)	OP7	OP6	OP5	OUT1	OUT2	R/G/B	VSYC	HSYC	00_{16}
ED_{16}	OSD clock selection register (CK)	0	0	0	0	0	0	CK1	CK0	00_{16}
EE_{16}	A-D control register 1 (AD1)				ADM4		ADM2	ADM1	ADM0	0 0 0 ? 0 0 0 0
EF_{16}	A-D control register 2 (AD2)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	00_{16}
$F0_{16}$	Timer 1 (TM1)									FF_{16}
$F1_{16}$	Timer 2 (TM2)									07_{16}
$F2_{16}$	Timer 3 (TM3)									FF_{16}
$F3_{16}$	Timer 4 (TM4)									07_{16}
$F4_{16}$	Timer 12 mode register (T12M)			0	T12M4	T12M3	T12M2	T12M1	T12M0	00_{16}
$F5_{16}$	Timer 34 mode register (T34M)			T34M5	T34M4	T34M3	T34M2	T34M1	T34M0	00_{16}
$F6_{16}$	PWM5 register (PWM5)									?
$F7_{16}$										?
$F8_{16}$										?
$F9_{16}$	Interrupt input polarity register (RE)	0		RE5	RE4	RE3	0	0		0 0 0 0 0 0 0 ?
FA_{16}	Test register (TEST)	00_{16}								00_{16}
FB_{16}	CPU mode register (CPUM)	1	1	1	1	1	CM2	0	0	1 1 1 1 1 1 0 0
FC_{16}	Interrupt request register 1 (IREQ1)	IT3R	IICR	VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	00_{16}
FD_{16}	Interrupt request register 2 (IREQ2)	0			MSR		S1R	1T2R	1T1R	00_{16}
FE_{16}	Interrupt control register 1 (ICON1)	IT3E	IICE	VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	00_{16}
FF_{16}	Interrupt control register 2 (ICON2)	0	0	0	MSE	0	S1E	1T2E	1T1E	00_{16}

Fig. 8.2.4 Memory Map of Special Function Register (SFR) (2)

■ 2 page register area (addresses 217_{16} to $21B_{16}$)

<Bit allocation>

- [ ] : } Function bit
- [Name] : } Function bit
- (shaded box) : No function bit
- [0] : Fix to this bit to "0" (do not write to "1")
- [1] : Fix to this bit to "1" (do not write to "0")

State immediately after reset>

- [0] : "0" immediately after reset
- [1] : "1" immediately after reset
- [?] : Indeterminate immediately after reset

Address	Register	b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset (b7–b0)
217_{16}	ROM correction address 1 (high-order)									00_{16}
218_{16}	ROM correction address 1 (low-order)									00_{16}
219_{16}	ROM correction address 2 (high-order)									00_{16}
$21A_{16}$	ROM correction address 2 (low-order)									00_{16}
$21B_{16}$	ROM correction enable register (RCR)	(no function)	(no function)	(no function)	(no function)	0	0	RCR1	RCR0	00_{16}

Note: Only M37221M4H/M6H/ M8H/MAH-XXXSP/FP and M37221EASP/FP have 2 page register.

Fig. 8.2.5 Memory Map of 2 Page Register Area

<Bit allocation>

- [ ] : / [Name] : } Function bit
- [shaded] : No function bit
- [0] (shaded) : Fix to this bit to "0" (do not write to "1")
- [1] (shaded) : Fix to this bit to "1" (do not write to "0")

<State immediately after reset>

- [0] : "0" immediately after reset
- [1] : "1" immediately after reset
- [?] : Indeterminate immediately after reset

Register	Bit allocation (b7 … b0)								State immediately after reset (b7 … b0)							
Processor status register (PS)	N	V	T	B	D	I	Z	C	?	?	?	?	?	1	?	?
Program counter (PCH)									Contents of address $FFFF_{16}$							
Program counter (PCL)									Contents of address $FFFE_{16}$							

Fig. 8.2.6 Internal State of Processor Status Register and Program Counter at Reset

8.3 INTERRUPTS

Interrupts can be caused by 14 different sources comprising 4 external, 8 internal, 1 software, and 1 reset interrupts. Interrupts are vectored interrupts with priorities as shown in Table 8.3.1. Reset is also included in the table as its operation is similar to an interrupt.
When an interrupt is accepted,

① The contents of the program counter and processor status register are automatically stored into the stack.
② The interrupt disable flag I is set to “1” and the corresponding interrupt request bit is set to “0.”
③ The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to “1.”
All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in Interrupt Request Registers 1 and 2 and the interrupt enable bits are in Interrupt Control Registers 1 and 2. Figures 8.3.2 to 8.3.6 show the interrupt-related registers.
Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is “1,” interrupt request bit is "1," and the interrupt disable flag is “0.”
The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to “0” and “1” by a program.
Reset is treated as a non-maskable interrupt with the highest priority.
Figure 8.3.1 shows interrupt controls.

8.3.1 Interrupt Causes

(1) VSYNC, OSD interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.
The OSD interrupt occurs after character block display to the CRT is completed.

(2) INT1 to INT3 external interrupts

The INT1 to INT3 interrupts are external interrupt inputs, the system detects that the level of a pin changes from LOW to HIGH or from HIGH to LOW, and generates an interrupt request. The input active edge can be selected by bits 3 to 5 of the interrupt input polarity register (address $00F9_{16}$) : when this bit is “0,” a change from LOW to HIGH is detected; when it is “1,” a change from HIGH to LOW is detected. Note that both bits are cleared to “0” at reset.

(3) Timers 1 to 4 interrupts

An interrupt is generated by an overflow of timers 1 to 4.

Table 8.3.1 Interrupt Vector Addresses and Priority

Priority	Interrupt Source	Vector Addresses	Remarks
1	Reset	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
2	OSD interrupt	$FFFD_{16}$, $FFFC_{16}$	
3	INT2 external interrupt	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
4	INT1 external interrupt	$FFF9_{16}$, $FFF8_{16}$	Active edge selectable
5	Timer 4 interrupt	$FFF5_{16}$, $FFF4_{16}$	
6	f(XIN)/4096 interrupt	$FFF3_{16}$, $FFF2_{16}$	
7	VSYNC interrupt	$FFF1_{16}$, $FFF0_{16}$	
8	Timer 3 interrupt	$FFEF_{16}$, $FFEE_{16}$	
9	Timer 2 interrupt	$FFED_{16}$, $FFEC_{16}$	
10	Timer 1 interrupt	$FFEB_{16}$, $FFEA_{16}$	
11	Serial I/O interrupt	$FFE9_{16}$, $FFE8_{16}$	
12	Multi-master I^{2}C-BUS interface interrupt	$FFE7_{16}$, $FFE6_{16}$	
13	INT3 external interrupt	$FFE5_{16}$, $FFE4_{16}$	Active edge selectable
14	BRK instruction interrupt	$FFDF_{16}$, $FFDE_{16}$	Non-maskable

(4) Serial I/O interrupt

This is an interrupt request from the clock synchronous serial I/O function.

(5) f(X_{IN})/4096 interrupt

The f (X_{IN})/4096 interrupt occurs regularly with a f(X_{IN})/4096 period. Set bit 0 of PWM output control register 1 to "0."

(6) Multi-master I^2C-BUS interface interrupt

This is an interrupt request related to the multi-master I^2C-BUS interface.

(7) BRK instruction interrupt

This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

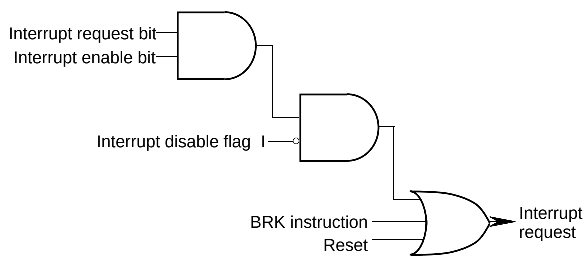


Fig. 8.3.1 Interrupt Control

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address $00FC_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	OSD interrupt request bit (CRTR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Multi-master I^2C-BUS interface interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	INT3 external interrupt request bit (IT3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻

✻: "0" can be set by software, but "1" cannot be set.

Fig. 8.3.2 Interrupt Request Register 1

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt request register 2 (IREQ2) [Address $00FD_{16}$]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (IT1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	INT2 external interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5, 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
7	Fix this bit to "0."		0	R	W

✻: "0" can be set by software, but "1" cannot be set.

Fig. 8.3.3 Interrupt Request Register 2

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address $00FE_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (CRTE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Multi-master I2C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	INT3 external interrupt enable bit (IT3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Fig. 8.3.4 Interrupt Control Register 1

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 _ 0 _ _ _

Interrupt control register 2 (ICON2) [Address $00FF_{16}$]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 external interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (S1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Fix this bit to "0."		0	R	W
4	f(XIN)/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5 to 7	Fix these bits to "0."		0	R	W

Fig. 8.3.5 Interrupt Control Register 2

Interrupt Input Polarity Register

b7	b6	b5	b4	b3	b2	b1	b0
0					0	0	

Interrupt input polarity register(RE) [Address 00F9$_{16}$]

B	Name	Functions	After reset	R	W
0	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
1,2	Fix These bits to “0.”		0	R	W
3	INT1 polarity switch bit (RE3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (RE4)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (RE5)	0 : Positive polarity 1 : Negative polarity	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
7	Fix this bit to “0.”		0	R	W

Fig. 8.3.6 Interrupt Input Polarity Register

8.4 TIMERS

This microcomputer has 4 timers: timers 1 to 4. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 8.4.3.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. By writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$: timers 1 to 4), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to “1” by a timer overflow at the next count pulse, after the count value reaches “00_{16}.”

8.4.1 Timer 1

Timer 1 can select one of the following count sources:

- $f(X_{IN})/16$
- $f(X_{IN})/4096$

The count source of timer 1 is selected by setting bit 0 of timer 12 mode register 1 (address $00F4_{16}$).

Timer interrupt request occurs at timer 1 overflow.

8.4.2 Timer 2

Timer 2 can select one of the following count sources:

- $f(X_{IN})/16$
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer 12 mode register (address $00F4_{16}$). When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

8.4.3 Timer 3

Timer 3 can select one of the following count sources:

- $f(X_{IN})/16$
- External clock from the HSYNC pin
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bits 5 and 0 of timer 34 mode register (address $00F5_{16}$).

Timer 3 interrupt request occurs at timer 3 overflow.

8.4.4 Timer 4

Timer 4 can select one of the following count sources:

- $f(X_{IN})/16$
- $f(X_{IN})/2$
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 1 and 4 of timer 34 mode register (address $00F5_{16}$). When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

At reset, timers 3 and 4 are connected by hardware and “FF_{16}” is automatically set in timer 3; “07_{16}” in timer 4. The $f(X_{IN})/16$ is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and “FF_{16}” is automatically set in timer 3; “07_{16}” in timer 4. However, the $f(X_{IN})/16$ is not selected as the timer 3 count source. So set both bit 0 of timer 34 mode register (address $00F5_{16}$) and bit 6 at address $00C7_{16}$ to “0” before execution of the STP instruction ($f(X_{IN})/16$ is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

The timer-related registers is shown in Figures 8.4.1 and 8.4.2.

Timer 12 Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register (T12M) [Address 00F4$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (T12M0)	0: f(XIN)/16 1: f(XIN)/4096	0	R	W
1	Timer 2 count source selection bit (T12M1)	0: Interrupt clock source 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (T12M2)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (T12M3)	0: Count start 1: Count stop	0	R	W
4	Timer 2 internal count source selection bit 2 (T12M4)	0: f(XIN)/16 1: Timer 1 overflow	0	R	W
5	Fix this bit to “0.”		0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.4.1 Timer 12 Mode Register

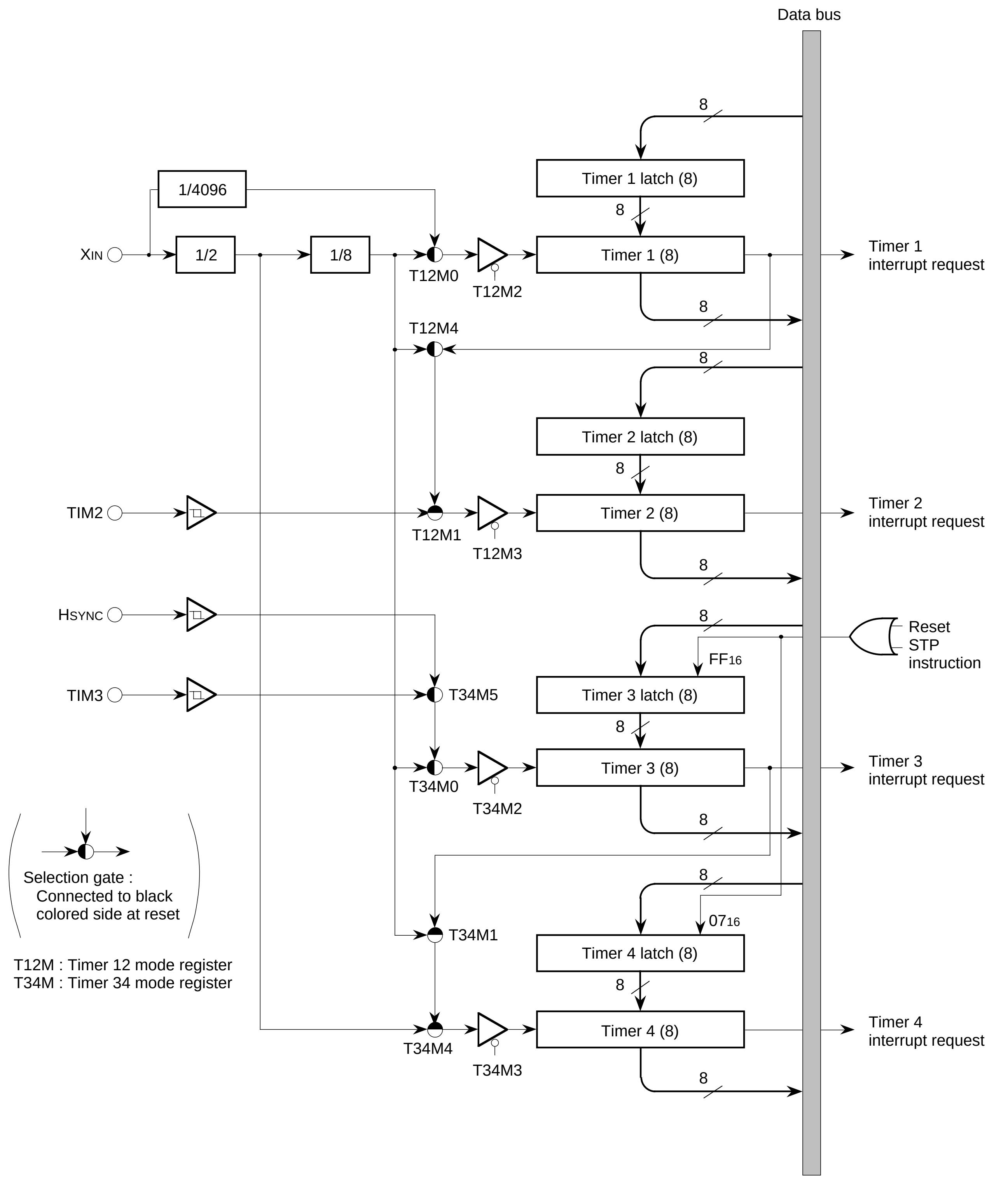
Timer 34 Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 34 mode register (T34M) [Address 00F5$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (T34M0)	0 : f(XIN)/16 1 : External clock source	0	R	W
1	Timer 4 internal interrupt count source selection bit (T34M1)	0 : Timer 3 overflow signal 1 : f(XIN)/16	0	R	W
2	Timer 3 count stop bit (T34M2)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (T34M3)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit (T34M4)	0: Internal clock source 1: f(XIN)/2	0	R	W
5	Timer 3 external count source selection bit (T34M5)	0: TIM3 pin input 1: HSYNC pin input	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.4.2 Timer 34 Mode Register



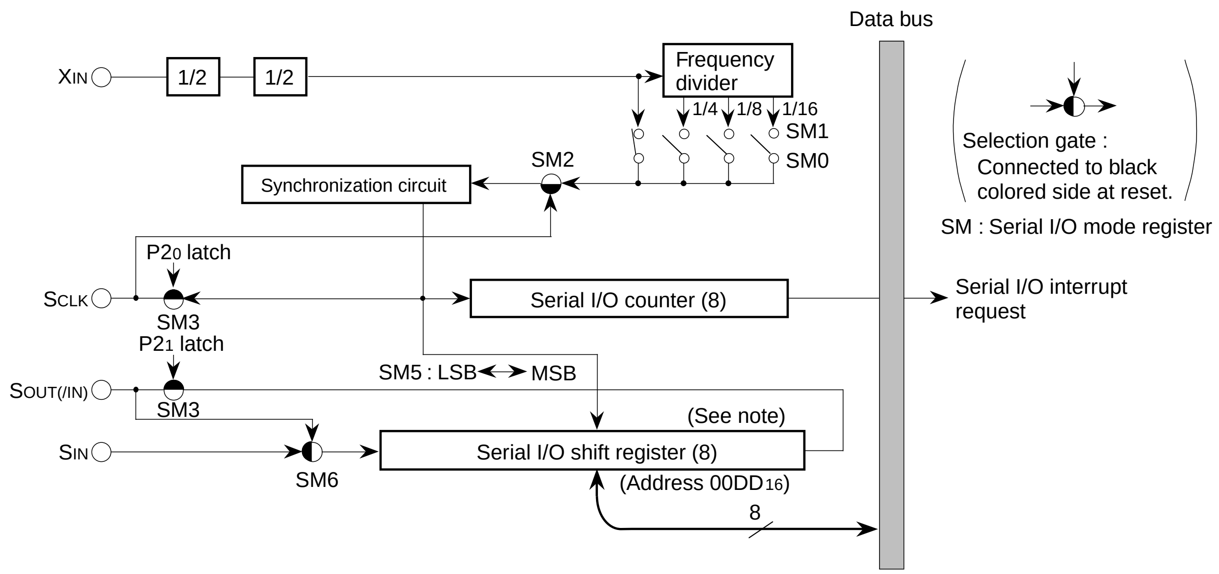
Notes 1: "H" pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2: When the external clock source is selected, timers 2 and 3 are counted at a rising edge of input signal.
3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 8.4.3 Timer Block Diagram

8.5 SERIAL I/O

This microcomputer has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.
The serial I/O block diagram is shown in Figure 8.5.1. The synchronous clock I/O pin (SCLK), data output pin (SOUT), and data input pin (SIN) also functions as port P2.
Bit 3 of the serial I/O mode register (address $00DC_{16}$) selects whether the synchronous clock is supplied internally or externally (from the SCLK pin). When an internal clock is selected, bits 1 and 0 select whether f(XIN) or f(XCIN) is divided by 4, 16, 32, or 64. To use SIN pin for serial I/O, set the corresponding bit of the port P2 direction register (address $00C5_{16}$) to "0."

The operation of the serial I/O is described below. The operation of the serial I/O differs depending on the clock source; external clock or internal clock.



Note : When the data is set in the serial I/O register (address $00DD_{16}$), the register functions as the serial I/O shift register.

Fig. 8.5.1 Serial I/O Block Diagram

Internal clock : The serial I/O counter is set to “7” during the write cycle into the serial I/O register (address $00DD_{16}$), and the transfer clock goes HIGH forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.
After the transfer clock has counted 8 times, the serial I/O counter becomes “0” and the transfer clock stops at HIGH. At this time the interrupt request bit is set to “1.”

External clock : The an external clock is selected as the clock source, the interrupt request is set to “1” after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 1 MHz or less with a duty cycle of 50%.
The serial I/O timing is shown in Figure 8.5.2. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.
2: When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.

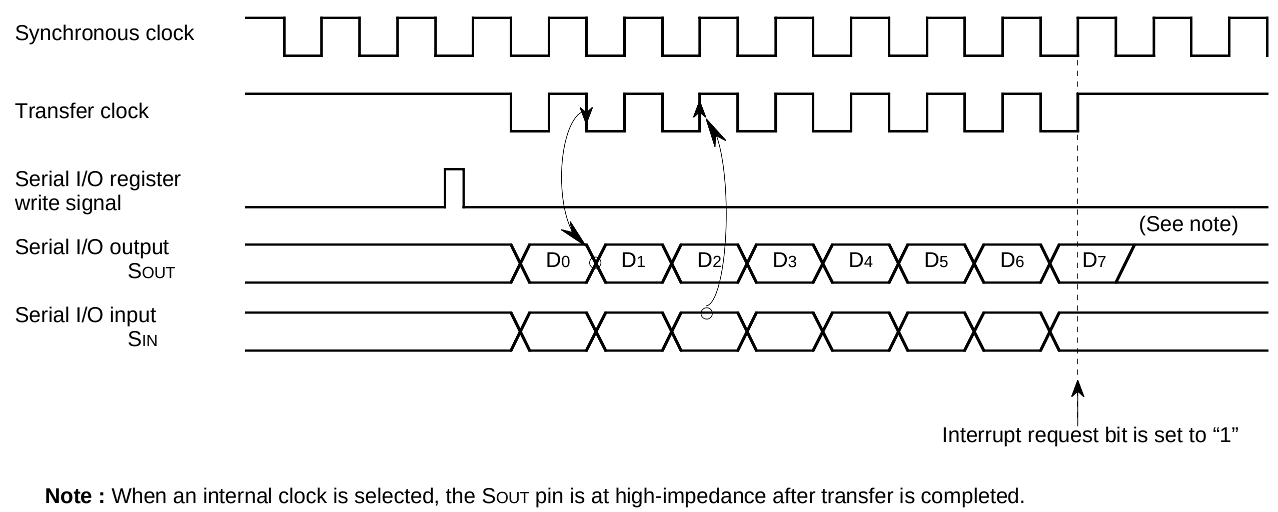


Fig. 8.5.2 Serial I/O Timing (for LSB first)

Serial I/O Mode Register

b7 b6 b5 b4 b3 b2 b1 b0 (b4 = 0)

Serial I/O mode register (SM) [Address $00DC_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(X_{IN})/4 0 1: f(X_{IN})/16 1 0: f(X_{IN})/32 1 1: f(X_{IN})/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Serial I/O port selection bit (SM3)	0: $P2_0$, $P2_1$ 1: S_{CLK}, S_{OUT}	0	R	W
4	Fix this bit to "0."		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Serial input pin selection bit (SM6)	0: Input signal from S_{IN} pin. 1: Input signal from S_{OUT} pin.	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 8.5.3 Serial I/O Mode Register

8.5.1 Serial I/O Common Transmission/Reception mode

By writing “1” to bit 6 of the serial I/O mode register, signals SIN and SOUT are switched internally to be able to transmit or receive the serial data.
Figure 8.5.4 shows signals on serial I/O common transmission/reception mode.

Note: When receiving the serial data after writing “FF_{16}” to the serial I/O register.

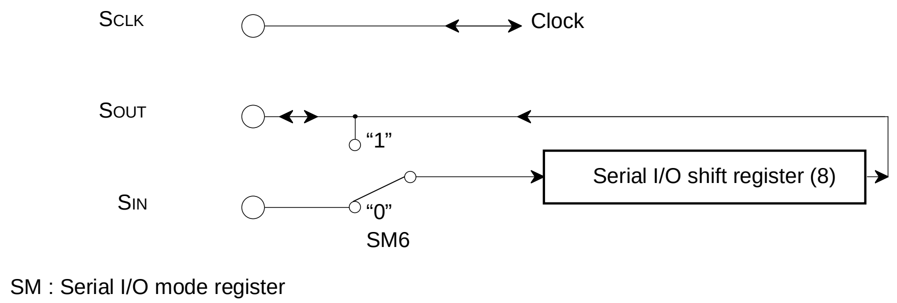


Fig. 8.5.4 Signals on Serial I/O Common Transmission/Reception Mode

8.6 MULTI-MASTER I^2C-BUS INTERFACE

The multi-master I^2C-BUS interface is a serial communications circuit, conforming to the Philips I^2C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.
Figure 8.6.1 shows a block diagram of the multi-master I^2C-BUS interface and Table 8.6.1 shows multi-master I^2C-BUS interface functions.
This multi-master I^2C-BUS interface consists of the I^2C address register, the I^2C data shift register, the I^2C clock control register, the I^2C control register, the I^2C status register and other control circuits.

Table 8.6.1 Multi-master I^2C-BUS Interface Functions

Item	Function
Format	In conformity with Philips I^2C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I^2C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ = 4 MHz)

ϕ : System clock = $f(X_{IN})/2$

Note : We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I^2C control register at address $00DA_{16}$) for connections between the I^2C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

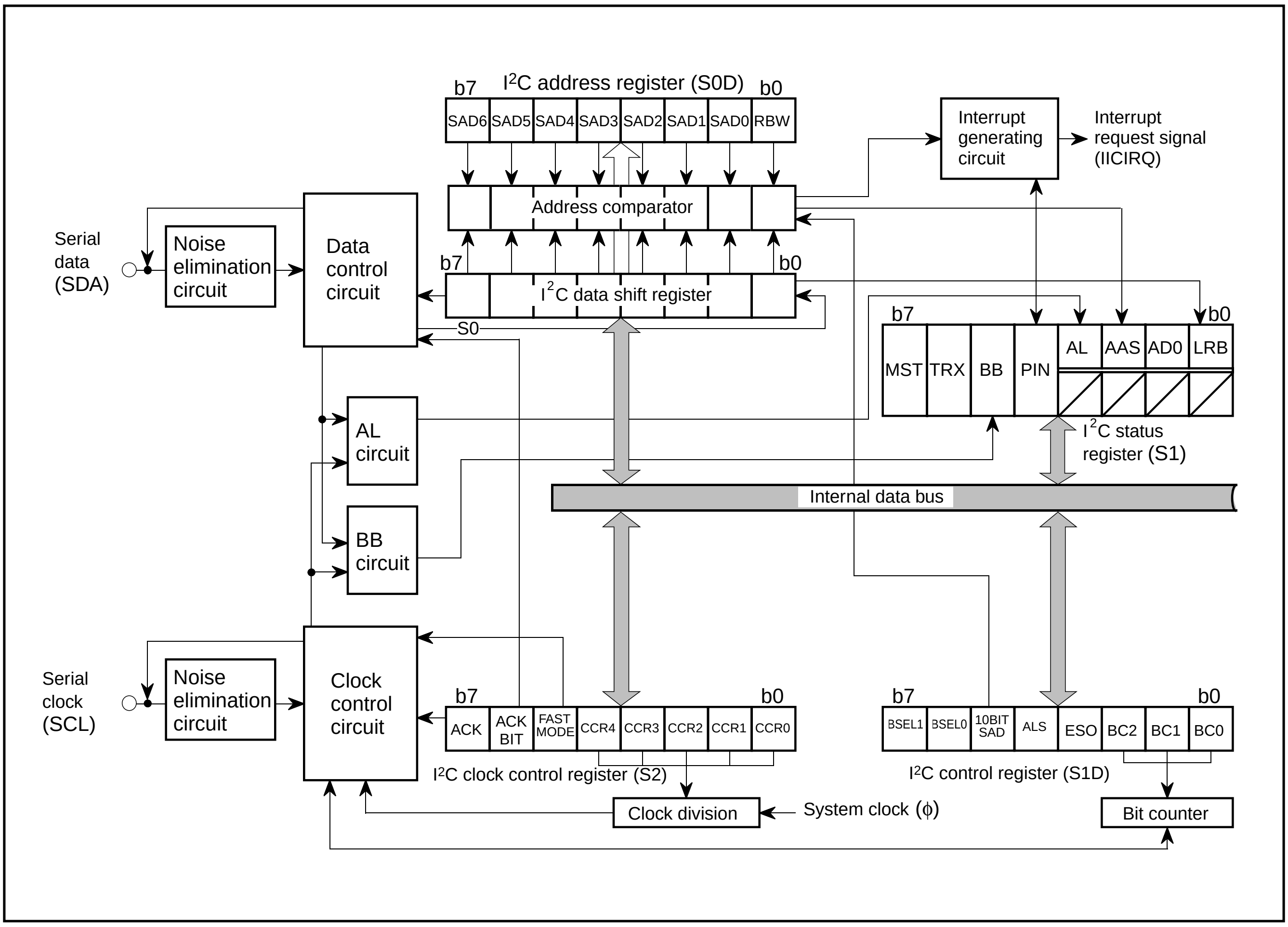


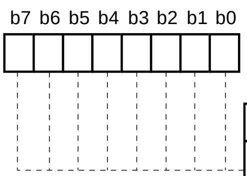
Fig. 8.6.1 Block Diagram of Multi-master I^2C-BUS Interface

8.6.1 I^{2}C Data Shift Register

The I^{2}C data shift register (S0 : address $00D7_{16}$) is an 8-bit shift register to store receive data and write transmit data.
When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.
The I^{2}C data shift register is in a write enable status only when the ESO bit of the I^{2}C control register (address $00DA_{16}$) is “1.” The bit counter is reset by a write instruction to the I^{2}C data shift register. When both the ESO bit and the MST bit of the I^{2}C status register (address $00D9_{16}$) are “1,” the SCL is output by a write instruction to the I^{2}C data shift register. Reading data from the I^{2}C data shift register is always enabled regardless of the ESO bit value.

Note: To write data into the I^{2}C data shift register after setting the MST bit to “0” (slave mode), keep an interval of 8 machine cycles or more.

I^{2}C Data Shift Register



I^{2}C data shift register (S0) [Address $00D7_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I^{2}C data shift register after setting the MST bit to “0” (slave mode), keep an interval of 8 machine cycles or more.

Fig. 8.6.2 Data Shift Register

8.6.2 I^{2}C Address Register

The I^{2}C address register (address 00D8_{16}) consists of a 7-bit slave address and a $\overline{\text{read}}$/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

(1) Bit 0: $\overline{\text{read}}$/write bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I^{2}C address register.
The RBW bit is cleared to “0” automatically when the stop condition is detected.

(2) Bits 1 to 7: slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

I^{2}C Address Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C address register (S0D) [Address 00D8_{16}]

B	Name	Functions	After reset	R	W
0	$\overline{\text{Read}}$/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Fig. 8.6.3 I^{2}C Address Register

8.6.3 I²C Clock Control Register

The I²C clock control register (address $00DB_{16}$) is used to set ACK control, SCL mode and SCL frequency.

(1) Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency.

(2) Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to “0,” the standard clock mode is set. When the bit is set to “1,” the high-speed clock mode is set.

(3) Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock✻ is generated. When this bit is set to “0,” the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to “1,” the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.
However, when the slave address matches the address data in the reception of address data at ACK BIT = “0,” the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

✻ACK clock: Clock for acknowledgement

(4) Bit 7: ACK clock bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to “0,” the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to “1,” the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission.The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmission. If data is written during transmission, the I²C clock generator is reset, so that data cannot be transmitted normally.

I²C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C clock control register (S2) [Address $00DB_{16}$]

B	Name	Functions			After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4–CCR0	Standard clock mode	High speed clock mode	0	R	W
		00 to 02	Setup disabled	Setup disabled			
		03	Setup disabled	333			
		04	Setup disabled	250			
		05	100	400 (See note)			
		06	83.3	166			
		⋮	500/CCR value	1000/CCR value			
		1D	17.2	34.5			
		1E	16.6	33.3			
		1F	16.1	32.3			
		(at ϕ = 4 MHz, unit : kHz)					
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R	W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R	W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
“0” period : “1” period = 3 : 2
In the other cases, the duty is as below.
“0” period : “1” period = 1 : 1

Fig. 8.6.4 I²C Address Register

8.6.4 I²C Control Register

The I²C control register (address $00DA_{16}$) controls the data communication format.

(1) Bits 0 to 2: bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.
When a START condition is received, these bits become "000_2" and the address data is always transmitted and received in 8 bits.

(2) Bit 3: I²C-BUS interface use enable bit (ESO)

This bit enables usage of the multimaster I²C BUS interface. When this bit is set to "0," interface is in the disabled status so the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.
When ESO = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (they are bits of the I²C status register at address $00D9_{16}$).
- Writing data to the I²C data shift register (address $00D7_{16}$) is disabled.

(3) Bit 4: data format selection bit (ALS)

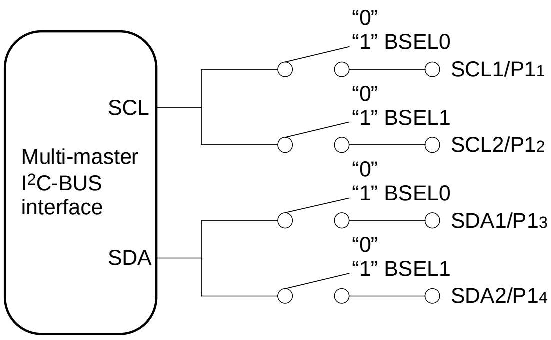
This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "8.6.5 I²C Status Register," bit 1) is received, transmission processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

(4) Bit 5: addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address $00D8_{16}$) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected and all the bits of the I²C address register are compared with the address data.

(5) Bits 6 and 7: connection control bits between I²C-BUS interface and ports (BSEL0, BSEL1)

These bits control the connection between SCL and ports or SDA and ports (refer to Figure 8.6.5).



Note: Set the corresponding direction register to "1" to use the port as multi-master I²C-BUS interface.

Fig. 8.6.5 Connection Port Control by BSEL0 and BSEL1

I2C Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I2C control register (S1D) [Address $00DA_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R	W
3	I2C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit(ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I2C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

Fig. 8.6.6 I2C Control Register

8.6.5 I²C Status Register

The I²C status register (address 00D9₁₆) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

(1) Bit 0: last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D7₁₆).

(2) Bit 1: general call detecting flag (AD0)

This bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

*General call: The master transmits the general call address "00₁₆" to all slaves.

(3) Bit 2: slave address comparison flag (AAS)

This flag indicates a comparison result of address data.

- In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in either of the following conditions.
  - The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I²C address register (address 00D8₁₆).
  - A general call is received.
- In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" in the following condition.
  - When the address data is compared with the I²C address register (8 bits consisting of slave address and RBW), the first bytes match.
- The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D7₁₆).

(4) Bit 3: arbitration lost* detecting flag (AL)

In the master transmission mode, when a device other than the microcomputer sets the SDA to "L,", arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

*Arbitration lost: The status in which communication as a master is disabled.

(5) Bit 4: I²C-BUS interface interrupt request bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When detecting the STOP condition in slave, the multi-master I²C-BUS interface interrupt request bit (IR) is set to "1" (interrupt request) regardless of falling of PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 8.6.8 shows an interrupt request signal generating timing chart.
The PIN bit is set to "1" in any one of the following conditions.

- Writing "1" to the PIN bit
- Executing a write instruction to the I²C data shift register (address 00D7₁₆) (See note)
- When the ESO bit is "0"
- At reset

Note: It takes 8 BCLK cycles or more until PIN bit becomes "1" after write instructions are executed to these registers.

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

(6) Bit 5: bus busy flag (BB)

This bit indicates the status of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (See note).
This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ESO bit of the I²C control register (address 00DA₁₆) is "0" at reset, the BB flag is kept in the "0" state.

(7) Bit 6: communication mode specification bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.
When the ALS bit of the I²C control register (address 00DA₁₆) is "0" in the slave reception mode, the TRX bit is set to "1" (transmit) if the least significant bit (R/$\overline{W}$ bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/$\overline{W}$ bit is "0," the TRX bit is cleared to "0" (receive).
The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication prevention function (Note).
- When MST = "0" and a START condition is detected.
- When MST = "0" and ACK non-return is detected.
- At reset

(8) Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification in data communications. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to "0" in any of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication prevention function (Note).
- At reset

Note: The START condition duplication prevention function disables the START condition generation, bit counter reset, and SCL output, when the following condition is satisfied:
a START condition is set by another master device.

I²C Status Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C status register (S1) [Address 00D9₁₆]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0 " 1 : Last bit = "1 " (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I²C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave recieve mode 0 1 : Slave transmit mode 1 0 : Master recieve mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannnot be written.

Fig. 8.6.7 I²C Status Register

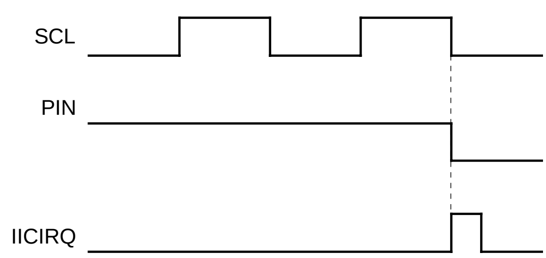


Fig. 8.6.8 Interrupt Request Signal Generation Timing

8.6.6 START Condition Generation Method

When the ESO bit of the I^2C control register (address $00DA_{16}$) is "1," execute a write instruction to the I^2C status register (address $00D9_{16}$) to set the MST, TRX and BB bits to "1." A START condition will then be generated. After that, the bit counter becomes "000_2" and an SCL is output for 1 byte . The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.9 for the START condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

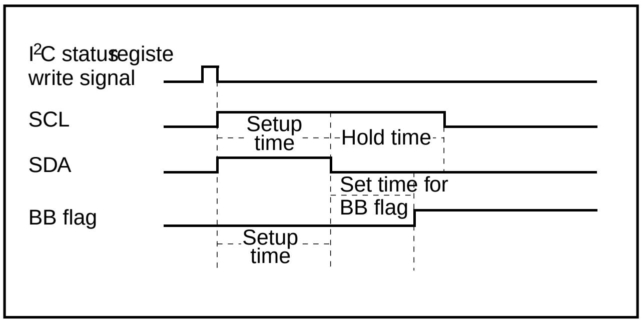


Fig. 8.6.9 START Condition Generation Timing Diagram

8.6.7 STOP Condition Generation Method

When the ESO bit of the I^2C control register (address $00DA_{16}$) is "1," execute a write instruction to the I^2C status register (address $00D9_{16}$) to set the MST bit and the TRX bit to "1" and the BB bit to "0". A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.10 for the STOP condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

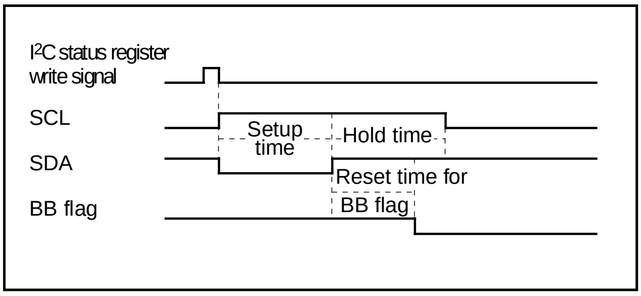


Fig. 8.6.10 STOP Condition Generation Timing Diagram

Table 8.6.2 START Condition/STOP Condition Generation Timing Table

Item	Standard Clock Mode	High-speed Clock Mode
Setup time (START condition)	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Setup time (STOP condition)	4.25 µs (17 cycles)	1.75 µs (7 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Set/reset time for BB flag	3.0 µs (12 cycles)	1.5 µs (6 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

8.6.8 START/STOP Condition Detect Conditions

The START/STOP condition detect conditions are shown in Figure 8.6.11 and Table 8.6.3. Only when the 3 conditions of Table 8.6.3 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal “IICIRQ” is generated to the CPU.

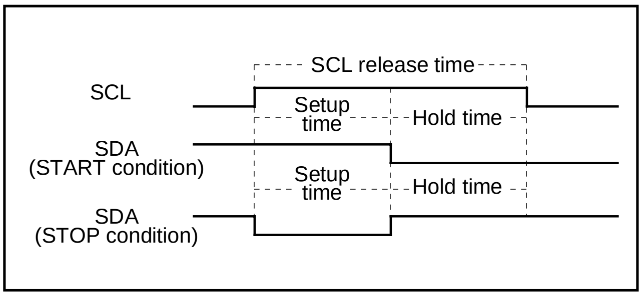


Fig. 8.6.11 START Condition/STOP Condition Detect Timing Diagram

Table 8.6.3 START Condition/STOP Condition Detect Conditions

Standard Clock Mode	High-speed Clock Mode
6.5 µs (26 cycles) < SCL release time	1.0 µs (4 cycles) < SCL release time
3.25 µs (13 cycles) < Setup time	0.5 µs (2 cycles) < Setup time
3.25 µs (13 cycles) < Hold time	0.5 µs (2 cycles) < Hold time

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

8.6.9 Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

(1) 7-bit addressing format

To support the 7-bit addressing format, set the 10BIT SAD bit of the I^{2}C control register (address $00DA_{16}$) to “0.” The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I^{2}C address register (address $00D8_{16}$). At the time of this comparison, address comparison of the RBW bit of the I^{2}C address register (address $00D8_{16}$) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 8.6.12, (1) and (2).

(2) 10-bit addressing format

To support the 10-bit addressing format, set the 10BIT SAD bit of the I^{2}C control register (address $00DA_{16}$) to “1.” An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I^{2}C address register (address $00D8_{16}$). At the time of this comparison, an address comparison is performed between the RBW bit of the I^{2}C address register (address $00D8_{16}$) and the R/$\overline{W}$ bit, which is the last bit of the address data transmitted from the master. In the 10-bit addressing mode, the R/$\overline{W}$ bit not only specifies the direction of communication for control data but is also processed as an address data bit.

When the first-byte address data matches the slave address, the AAS bit of the I^{2}C status register (address $00D9_{16}$) is set to “1.” After the second-byte address data is stored into the I^{2}C data shift register (address $00D7_{16}$), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd byte matches the slave address, set the RBW bit of the I^{2}C address register (address $00D8_{16}$) to “1” by software. This processing can match the 7-bit slave address and R/$\overline{W}$ data, which are received after a RESTART condition is detected, with the value of the I^{2}C address register (address $00D8_{16}$). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 8.6.12, (3) and (4).

8.6.10 Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz with the ACK return mode enable, is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $00D8_{16}$) and “0” in the RBW bit.
② Set the ACK return mode and SCL = 100 kHz by setting “85_{16}” in the I^2C clock control register (address $00DB_{16}$).
③ Set “10_{16}” in the I^2C status register (address $00D9_{16}$) and hold the SCL at HIGH.
④ Set a communication enable status by setting “48_{16}” in the I^2C control register (address $00DA_{16}$).
⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address $00D7_{16}$) and set “0” in the least significant bit.
Set “$F0_{16}$” in the I^2C status register (address $00D9_{16}$) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
⑦ Set transmit data in the I^2C data shift register (address $00D7_{16}$). At this time, an SCL and an ACK clock automatically occurs.
⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
⑨ Set “$D0_{16}$” in the I^2C status register (address $00D9_{16}$). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

8.6.11 Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, with the ACK non-return mode enabled while using the addressing format, is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $00D8_{16}$) and “0” in the RBW bit.
② Set the ACK non-return mode and SCL = 400 kHz by setting “25_{16}” in the I^2C clock control register (address $00DB_{16}$).
③ Set “10_{16}” in the I^2C status register (address $00D9_{16}$) and hold the SCL at HIGH.
④ Set a communication enable status by setting “48_{16}” in the I^2C control register (address $00DA_{16}$).
⑤ When a START condition is received, an address comparison is executed.
•When all transmitted address are“0” (general call):
AD0 of the I^2C status register (address $00D9_{16}$) is set to “1” and an interrupt request signal occurs.
•When the transmitted addresses match the address set in ①:
ASS of the I^2C status register (address $00D9_{16}$) is set to “1” and an interrupt request signal occurs.
•In the cases other than the above:
AD0 and AAS of the I^2C status register (address $00D9_{16}$) are set to “0” and no interrupt request signal occurs.
⑦ Set dummy data in the I^2C data shift register (address $00D7_{16}$).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

S	Slave address	R/$\overline{W}$	A	Data	A	Data	A/$\overline{A}$	P
	7 bits	"0"		1 to 8 bits		1 to 8 bits		

(1) A master-transmitter transmits data to a slave-receiver

S	Slave address	R/$\overline{W}$	A	Data	A	Data	$\overline{A}$	P
	7 bits	"1"		1 to 8 bits		1 to 8 bits		

(2) A master-receiver receives data from a slave-transmitter

S	Slave address 1st 7 bits	R/$\overline{W}$	A	Slave address 2nd byte	A	Data	A	Data	A/$\overline{A}$	P
	7 bits	"0"		8 bits		1 to 8 bits		1 to 8 bits		

(3) A master-transmitter transmits data to a slave-receiver with a 10-bit address

S	Slave address 1st 7 bits	R/$\overline{W}$	A	Slave address 2nd byte	A	Sr	Slave address 1st 7 bits	R/$\overline{W}$	Data	A	Data	$\overline{A}$	P
	7 bits	"0"		8 bits			7 bits	"1"	1 to 8 bits		1 to 8 bits		

(4) A master-receiver receives data from a slave-transmitter with a 10-bit address

S : START condition
A : ACK bit
Sr : Restart condition
P : STOP condition
R/$\overline{W}$: Read/$\overline{\text{Write}}$ bit
(shaded) From master to slave
(unshaded) From slave to master

Fig. 8.6.12 Address Data Communication Format

8.6.12 Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

Precautions for executing the read-modify-write instructions such as SEB, and CLB, is for each register of the multi-master I²C-BUS interface are described below.

•I²C data shift register (S0)
When executing the read-modify-write instruction for this register during transfer, data may become an arbitrary value.

•I²C address register (S0D)
When the read-modify-write instruction is executed for this register at detection of the STOP condition, data may become an arbitrary value. It is because hardware changes the $\overline{\text{read}}$/write bit (RBW) at the timing.

•I²C status register (S1)
Do not execute the read-modify-write instruction for this register because all bits of this register are changed by hardware.

•I²C control register (S1D)
When the read-modify-write instruction is executed for this register at detection of the START condition or at completion the byte transfer, data may become an arbitrary value. Because hardware changes the bit counter (BC0–BC2) at the timing.

•I²C clock control register (S2)
The read-modify-write instruction can be executed for this register.

(2) START condition generation procedure using multi-master

① Procedure example (The necessary conditions for the procedure are described in ② to ⑤ below).

```
          •
          •
     LDA       —                 (Take out slave address value)
     SEI                         (Interrupt disabled)
     BBS  5,S1,BUSBUSY           (BB flag confirmation and branch process)
BUSFREE:
     STA  S0                     (Write slave address value)
     LDM  #$F0, S1               (Trigger START condition generation)
     CLI                         (Interrupt enabled)
          •
          •
BUSBUSY:
     CLI                         (Interrupt enabled)
          •
          •
```

② Use "STA," "STX" or "STY" of the zero page addressing instruction for writing the slave address value to the I²C data shift register.

③ Use "LDM" instruction for setting trigger of START condition generation.

④ Write the slave address value of ② and set trigger of START condition generation as in ③ continuously as shown in the procedure example.

⑤ Disable interrupts during the following three process steps:
- BB flag confirmation
- Write of slave address value
- Trigger of START condition generation

When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generation procedure

①Procedure example (The necessary conditions for the procedure are described in ② to ⑥ below.)

Execute the following procedure when the PIN bit is “0.”

```
        •
        •
LDM  #$00, S1    (Select slave receive mode)
LDA  —           (Take out slave address value)
SEI              (Interrupt disabled)
STA  S0          (Write slave address value)
LDM  #$F0, S1    (Trigger RESTART condition generation)
CLI              (Interrupt enabled)
        •
        •
```

② Select the slave receive mode when the PIN bit is “0.” Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.
The TRX bit becomes “0” and the SDA pin is released.

③ The SCL pin is released by writing the slave address value to the I^{2}C data shift register. Use “STA,” “STX” or “STY” of the zero page addressing instruction for writing.

④ Use “LDM” instruction for setting trigger of RESTART condition generation.

⑤ Write the slave address value of ③ and set trigger of RESTART condition generation of ④ continuously, as shown in the procedure example.
Disable interrupts during the following two process steps:
- Write slave address value
- Trigger RESTART condition generation

(4) STOP condition generation procedure

①Procedure example (The necessary conditions for the procedure are described in ② to ④ below.)

```
        •
        •
SEI              (Interrupt disabled)
LDM  #$C0, S1    (Select master transmit mode)
NOP              (Set NOP)
LDM  #$D0, S1    (Trigger STOP condition generation)
CLI              (Interrupt enabled)
        •
        •
```

② Write “0” to the PIN bit when master transmit mode is selected.

③ Execute “NOP” instruction after master transmit mode is set. Also, set trigger of STOP condition generation within 10 cycles after selecting the master trasmit mode.

④ Disable interrupts during the following two process steps:
- Select master transmit mode
- Trigger STOP condition generation

(5) Writing to I^{2}C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously as it may cause the SCL pin the SDA pin to be released after about one machine cycle. Also, do not execute an instruction to set the MST and TRX bits to “0” from “1” when the PIN bit is “1,” as it may cause the same problem.

(6) Process after STOP condition generation

Do not write data in the I^{2}C data shift register S0 and the I^{2}C status register S1 until the bus busy flag BB becomes “0” after generation the STOP condition in the master mode. Doing so may cause the STOP condition waveform from being generated normally. Reading the registers does not cause the same problem.

8.7 PWM OUTPUT FUNCTION

This microcomputer is equipped with two 14-bit PWM (DA) and six 8-bit PWMs (PWM0–PWM5). DA1 and DA2 have a 14-bit resolution with the minimum resolution bit width of 0.25 µs and a repeat period of 4096 µs (for $f(X_{IN})$ = 8 MHz). PWM0–PWM7 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 µs and repeat period of 1024 µs (for $f(X_{IN})$ = 8 MHz).
Figure 8.7.1 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to DA and PWM0–PWM5 using $f(X_{IN})$ divided by 2 as a reference signal.

8.7.1 Data Setting

When outputting DA, first set the high-order 8 bits to the DA-H register (address $00CE_{16}$), then the low-order 6 bits to the DA-L register (address $00CF_{16}$). When outputting PWM0–PWM5, set 8-bit output data to the PWMi register (i means 0 to 5; addresses $00D0_{16}$ to $00D4_{16}$, $00F6_{16}$).

8.7.2 Transferring Data from Registers to PWM Circuit

Data transfer from the 8-bit PWM register to the 8-bit PWM circuit is executed when writing data to the register.
The signal output from the 8-bit PWM output pin corresponds to the contents of this register.
Also, data transfer from the DA register (addresses $00CE_{16}$ and $00CF_{16}$) to the 14-bit PWM circuit is executed at writing data to the DA-L register (address $00CF_{16}$). Reading from the DA-H register (address $00CE_{16}$) means reading this transferred data. Accordingly, it is possible to confirm the data being output from the DA output pin by reading the DA register.

8.7.3 Operating of 8-bit PWM

The following explains the PWM operation.
First, set bit 0 of PWM output control register 1 (address $00D5_{16}$) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied.
PWM0–PWM5 are also used as ports $P0_0$–$P0_5$, respectively. Set those of the port P0 direction register to "1." And select each output polarity by bit 3 of PWM output control register 2 (address $00D6_{16}$). Then, set bits 2 to 7 of PWM output control register 1 to "1" (PWM output).
The PWM waveform is output from the PWM output pins by setting these registers.
Figure 8.7.2 shows the 8-bit PWM timing. One cycle (T) is composed of 256 (2^8) segments. 8 kinds of pulses, relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 8.7.2 (a). The 8-bit PWM outputs a waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 8.7.2 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. An entirely HIGH selection cannot be output, i.e. 256/256.

8.7.4 Operating of 14-bit PWM

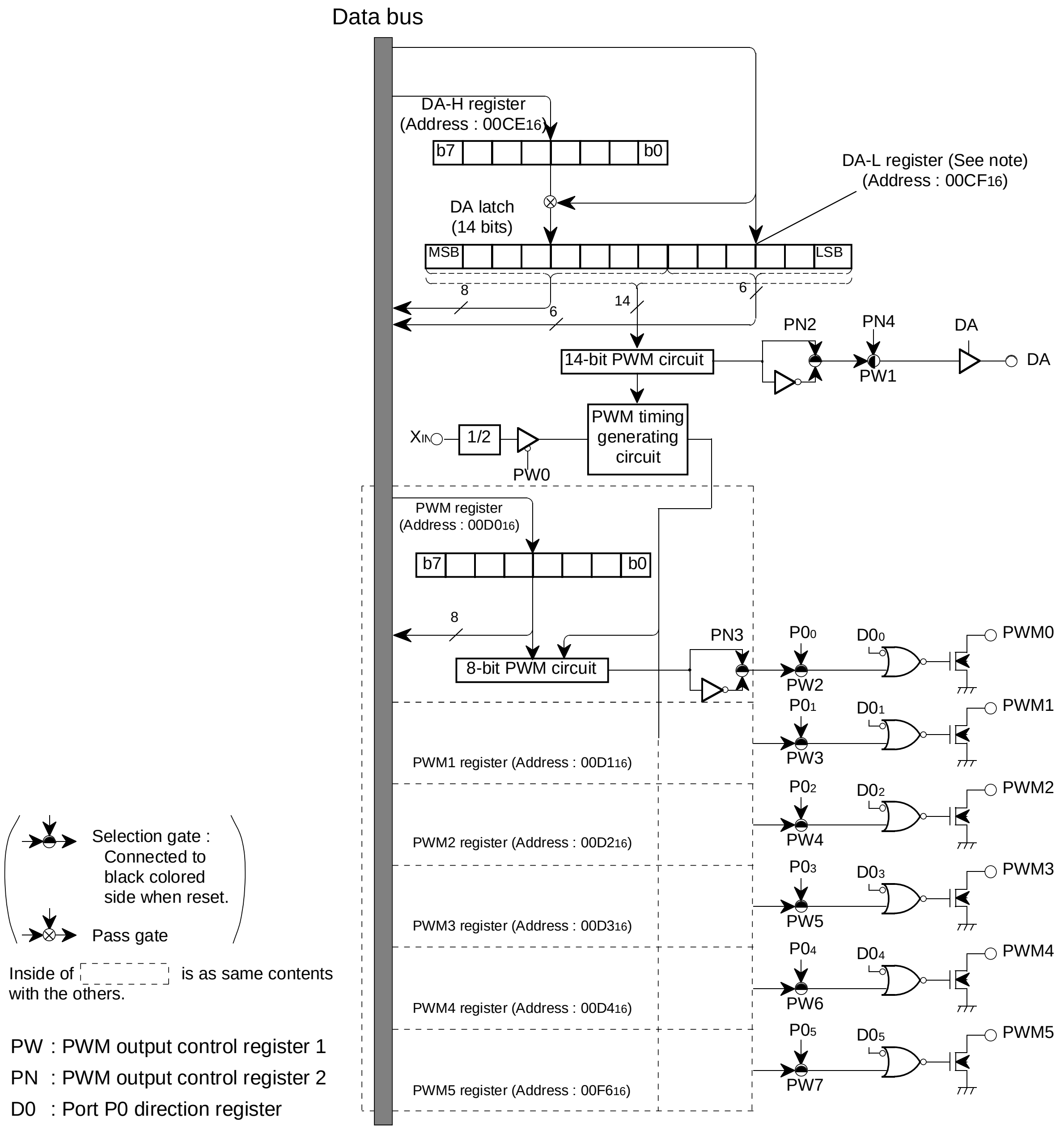
As with 8-bit PWM, set the bit 0 of PWM output control register 1 (address $00D5_{16}$) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied. Next, select the output polarity by bit 2 of PWM output control register 2 (address $00D6_{16}$). Then, the 14-bit PWM outputs from the D-A output pin by setting bit 1 of PWM output control register 1 to "0" (at reset, this bit already set to "0" automatically) to select the DA output.
The output example of the 14-bit PWM is shown in Figure 8.7.3.
The 14-bit PWM divides the data of the DA latch into the low-order 6 bits and the high-order 8 bits.
The fundamental waveform is determined with the high-order 8-bit data "D_H." A HIGH area with a length t × D_H (HIGH area of fundamental waveform) is output every short area of "t" = 256τ = 64 µs (τ is the minimum resolution bit width of 250 ns). The HIGH level area increase interval (t_m) is determined with the low-order 6-bit data "D_L." The HIGH are of smaller intervals "t_m" shown in Table 5 is longer by t than that of other smaller intervals in PWM repeat period "T" = 64t. Thus, a rectangular waveform with the different HIGH width is output from the DA pins. Accordingly, the PWM output changes by τ unit pulse width by changing the contents of the DA-H and DA-L registers. A length of entirely HIGH cannot be output, i. e. 256/256.

8.7.5 Output after Reset

At reset, the output of ports $P0_0$–$P0_5$ are in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

Table 8.7.1 Relation Between the Low-order 6-bit Data and High-level Area Increase Interval

Low-order 6 bits of Data	Area Longer by τ than That of Other t_m (m = 0 to 63)
0 0 0 0 0 0 (LSB)	Nothing
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ... 57, 59, 61, 63



Note: The DA-L register also functions as the low-order 6 bits of the DA latch.

Fig. 8.7.1 PWM Block Diagram

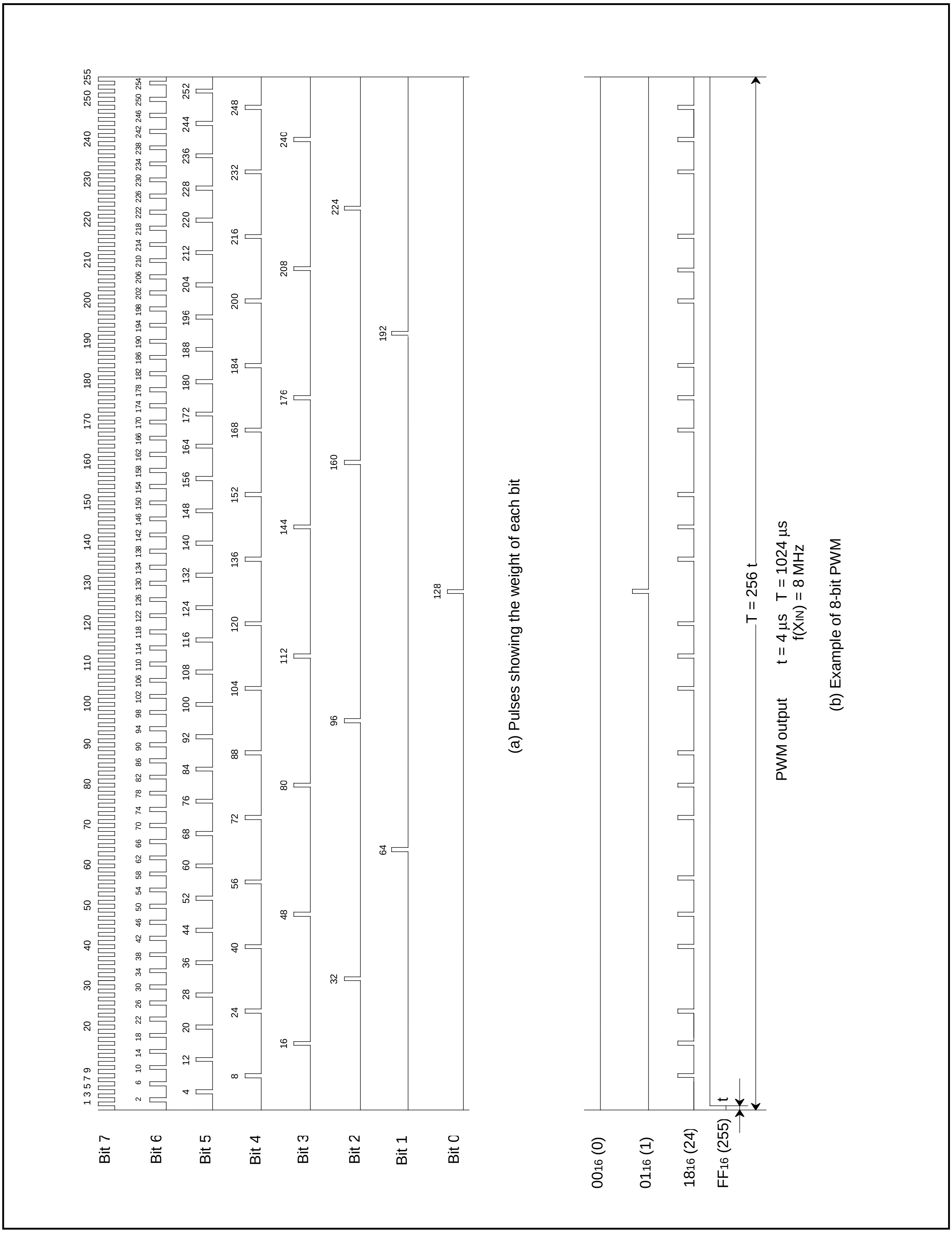


Fig. 8.7.2 PWM Timing

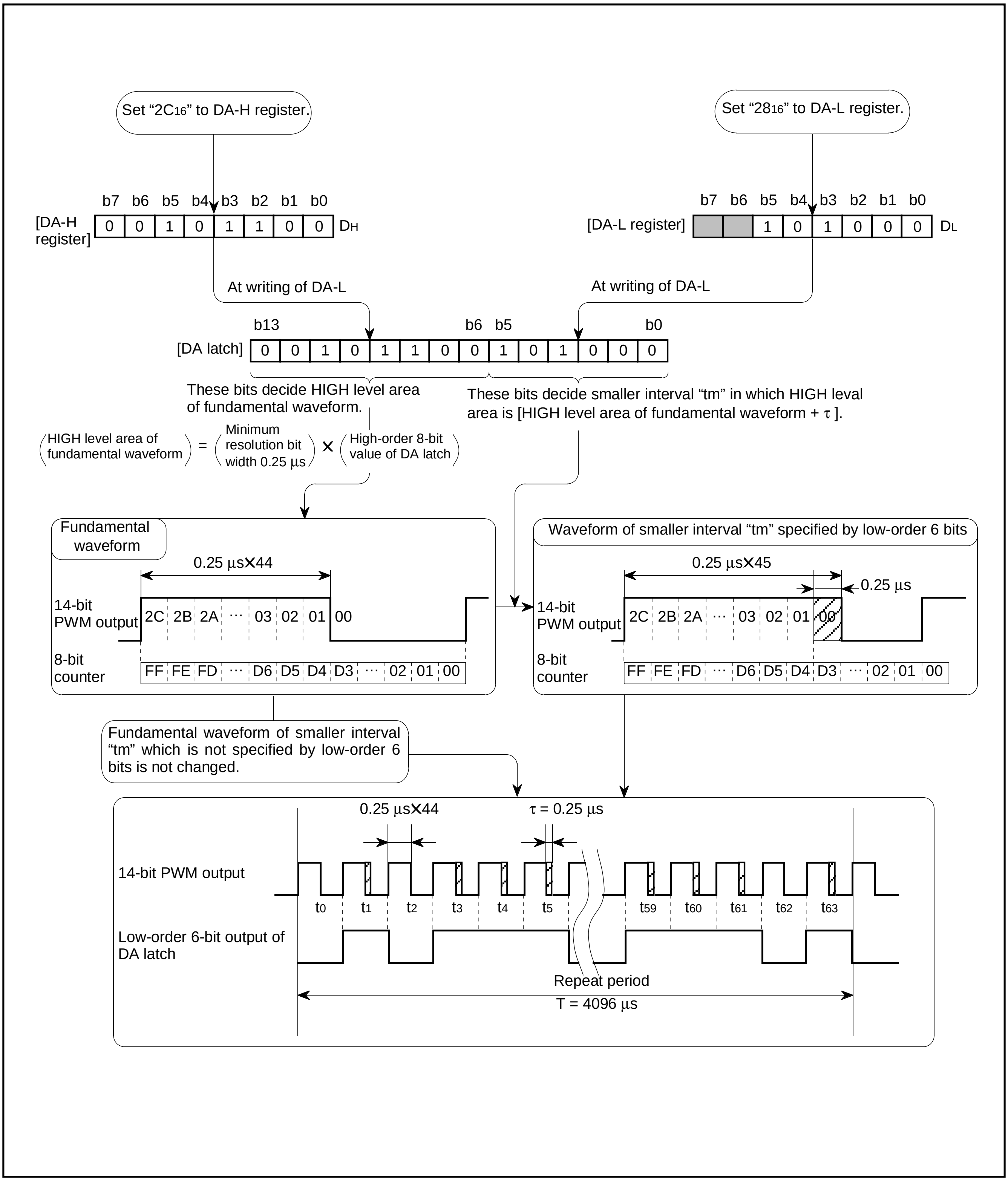


Fig. 8.7.3 14-bit PWM Timing (f(XIN) = 8 MHz)

PWM Output Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

PWM output control register 1 (PW) [Address $00D5_{16}$]

B	Name	Functions	After reset	R	W
0	DA, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA/PN4 selection bit (PW1)	0 : DA output 1 : PN4 output	0	R	W
2	$P0_0$/PWM0 output selection bit (PW2)	0: $P0_0$ output 1: PWM0 output	0	R	W
3	$P0_1$/PWM1 output selection bit (PW3)	0: $P0_1$ output 1: PWM1 output	0	R	W
4	$P0_2$/PWM2 output selection bit (PW4)	0: $P0_2$ output 1: PWM2 output	0	R	W
5	$P0_3$/PWM3 output selection bit (PW5)	0: $P0_3$ output 1: PWM3 output	0	R	W
6	$P0_4$/PWM4 output selection bit (PW6)	0: $P0_4$ output 1: PWM4 output	0	R	W
7	$P0_5$/PWM5 output selection bit (PW7)	0: $P0_5$ output 1: PWM5 output	0	R	W

Fig. 8.7.4 PWM Output Control Register 1

PWM Output Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

PWM output control register 2 (PN) [Address $00D6_{16}$]

B	Name	Functions	After reset	R	W
0,1	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
2	DA output polarity selection bit (PN2)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA general-purpose output bit (PN4)	0 : Output LOW 1 : Output HIGH	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.7.5 PWM Output Control Register 2

8.8 A-D COMPARATOR

A-D comparator consists of a 6-bit D-A converter and a comparator. The A-D comparator block diagram is shown in Figure 8.8.1.
The reference voltage "V_{ref}" for D-A conversion is set by bits 0 to 5 of the A-D control register 2 (address $00EF_{16}$).
The comparison result of the analog input voltage and the reference voltage "V_{ref}" is stored in bit 4 of the A-D control register 1 (address $00EE_{16}$).
For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data to select analog input pins for bits 0 to 2 of the A-D control register 1 and write the digital value corresponding to V_{ref} to be compared to bits 0 to 5 of the A-D control register 2. The voltage comparison is started by writing to the A-D control register 2, and it is completed after 16 machine cycles (NOP instruction ✕ 8).

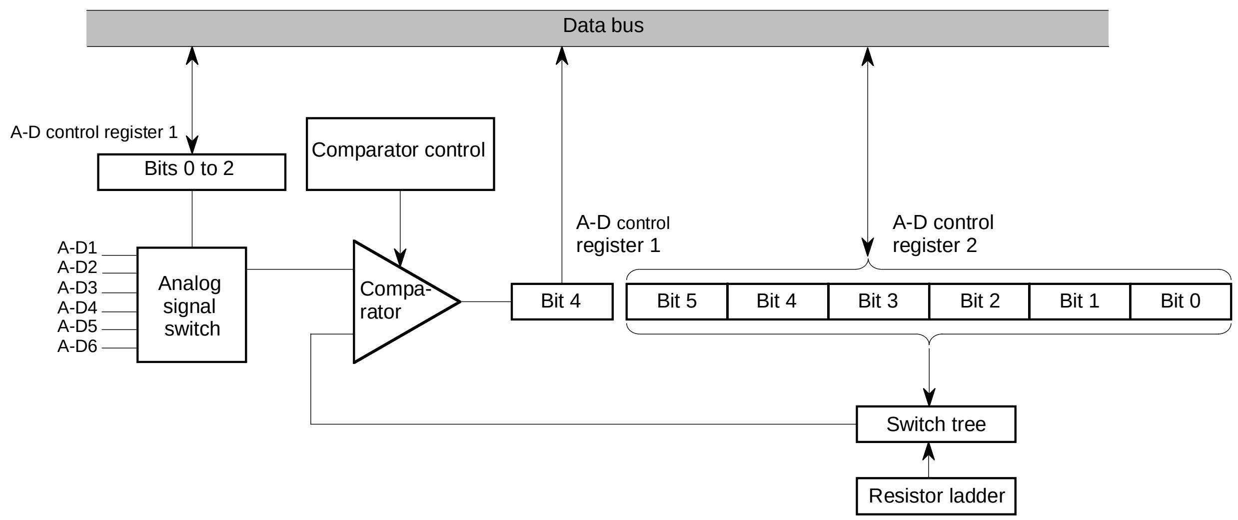


Fig. 8.8.1 A-D Comparator Block Diagram

A-D Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

A-D control register 1 (AD1) [Address 00EE16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADM0 to ADM2)	b2 b1 b0 0 0 0 : A-D1 0 0 1 : A-D2 0 1 0 : A-D3 0 1 1 : A-D4 1 0 0 : A-D5 1 0 1 : A-D6 1 1 0 : Do not set 1 1 1 : Do not set	0	R	W
3	This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	—
5 to 7	Nothing is assigned. This bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.8.2 A-D Control Register 1

A-D Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

A-D control register 2 (AD2) [Address 00EF16]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC0 to ADC5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc ⋮ 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are reed out, the values are “ 0.”		0	R	—

Fig. 8.8.3 A-D Control Register 2

8.9 D-A CONVERTER

This microcomputer has 2 D-A converters with 6-bit resolution. D-A converter block diagram is shown in Figure 8.9.1.
D-A conversion is performed by setting the value in the DA conversion register. The result of D-A conversion is output from the DA pin by setting “1” to the DA output enable bit of the port P3 output mode control register (bits 2 and 3 at address $00CD_{16}$).
The output analog voltage V is determined with the value n (n: decimal number) in the DA conversion register.

$$V = V_{CC} \times \frac{n}{64} \quad (n = 0 \text{ to } 63)$$

The DA output does not build in a buffer, so connect an external buffer when driving a low-impedance load.

Note: Only M37221EASP/FP have a built-in D-A converter.

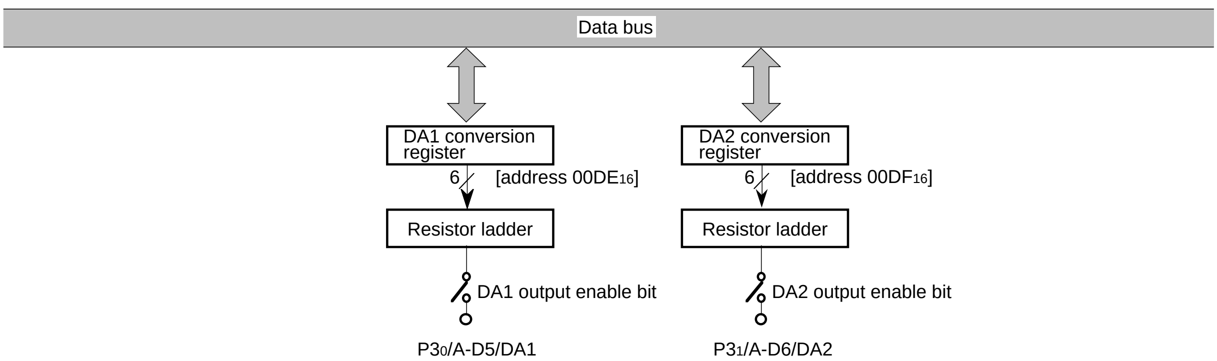


Fig. 8.9.1 D-A converter block diagram

P3 output mode control register

b7 b6 b5 b4 b3 b2 b1 b0

P3 output mode control register(P3S) [Address $00CD_{16}$]

B	Name	Functions	After reset	R	W
0	$P3_0$ output form selection bit (P30S)	0: CMOS output 1: N-channel open-drain output	0	R	W
1	$P3_1$ output form selection bit (P31S)	0: CMOS output 1: N-channel open-drain output	0	R	W
2	DA1 output enable bit (DA1S)	0: $P3_0$ input/output 1: DA1 output	0	R	W
3	DA2 output enable bit (DA2S)	0: $P3_1$ input/output 1: DA2 output	0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.9.2 P3 output mode control register

DA conversion register i

b7 b6 b5 b4 b3 b2 b1 b0 (b6: 0)

DA conversion register i (i=1, 2) (DAi) [Addresses $00DE_{16}$, $00DF_{16}$]

B	Name	Functions	After reset	R	W
0 to 5	DA conversion selection bit (DAi0 to DAi5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 0/64Vcc 0 0 0 0 0 1 : 1/64Vcc 0 0 0 0 1 0 : 2/64Vcc ⋮ 1 1 1 1 0 1 : 61/64Vcc 1 1 1 1 1 0 : 62/64Vcc 1 1 1 1 1 1 : 63/64Vcc	0	R	W
6	Fix this bit to “0.”		0	R	W
7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Note : When use M37221M4H/M6H/M8H/MAH-XXXSP/FP, there is not this register. Fix to “ 00_{16}.”

Fig. 8.9.3 DA conversion register i (i = 1, 2)

8.10 ROM CORRECTION FUNCTION

This can correct program data in the ROM. Up to 2 addresses can be corrected ; a program for correction is stored in the ROM correction memory in the RAM as the top address. There are 2 vectors for ROM correction :

Vector 1 : address $02C0_{16}$

Vector 2 : address $02E0_{16}$

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the top address of the ROM correction vector, the main program branches to the correction program stored in the ROM memory. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. The ROM correction function is controlled by the ROM correction enable register.

Notes 1: Specify the first address (op code address) of each instruction as the ROM correction address.

2: Use the JMP instruction (total of 3 bytes) to return from the correction program to the main program.

3: Do not set the same ROM correction address to both vectors 1 and 2.

ROM correction address 1 (high-order)	0217_{16}
ROM correction address 1 (low-order)	0218_{16}
ROM correction address 2 (high-order)	0219_{16}
ROM correction address 2 (low-order)	$021A_{16}$

Fig. 8.10.1 ROM Correction Address Registers

ROM Correction Enable Register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0		

ROM correction enable register (RCR) [Address $021B_{16}$]

B	Name	Functions	After reset	R	W
0	Vector 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Vector 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to “0.”		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.10.2 ROM Correction Enable Register

8.11 OSD FUNCTIONS

Table 8.11.1 outlines the OSD functions. This microcomputer incorporates an OSD control circuit of 24 characters ✕ 2 lines. OSD is controlled by the CRT control register. Up to 256 kinds of characters can be displayed. The colors can be specified for each character and up to 4 kinds of colors can be displayed on one screen. A combination of up to 8 colors can be obtained by using each output signal (R, G, and B).

Characters are displayed in a 12 ✕ 16 dots configuration to obtain smooth character patterns (refer to Figure 8.11.1).

The following shows the procedure how to display characters on the CRT screen.

① Write the display character code in OSD RAM.
② Specify the display color by using the color register.
③ Write the color register in which the display color is set in OSD RAM.
④ Specify the vertical position by using the vertical position register.
⑤ Specify the character size by using the character size register.
Specify the horizontal position by using the horizontal position register.
⑦ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the OSD starts according to the input of the VSYNC signal.

Table 8.11.1 Features of Each Display Mode

Parameter	Functions
Number of display characters	24 characters ✕ 2 lines
Dot structure	12 ✕ 16 dots
Kinds of characters	256 kinds
Kinds of character sizes	3 kinds
Attribute	Border (black)
Character font coloring	1 screen : 8 kinds (per character unit)
Character background coloring	1 screen : 8 kinds (per character unit)
OSD output	R, G, B
Display position	Horizontal: 64 levels, Vertical: 128 levels
Display expansion (multiline display)	Possible

The OSD circuit has an extended display mode. This mode allows multiple lines (3 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display has been terminated by software.
Figure 8.11.1 shows the configuration of an OSD character. Figure 8.11.2 shows the block diagram of the OSD circuit. Figure 8.11.3 shows OSD control register.

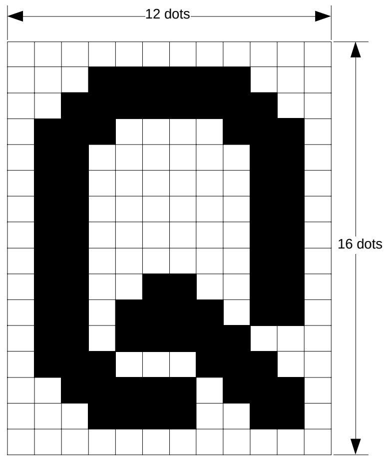


Fig. 8.11.1 Configuration of OSD Character Display Area

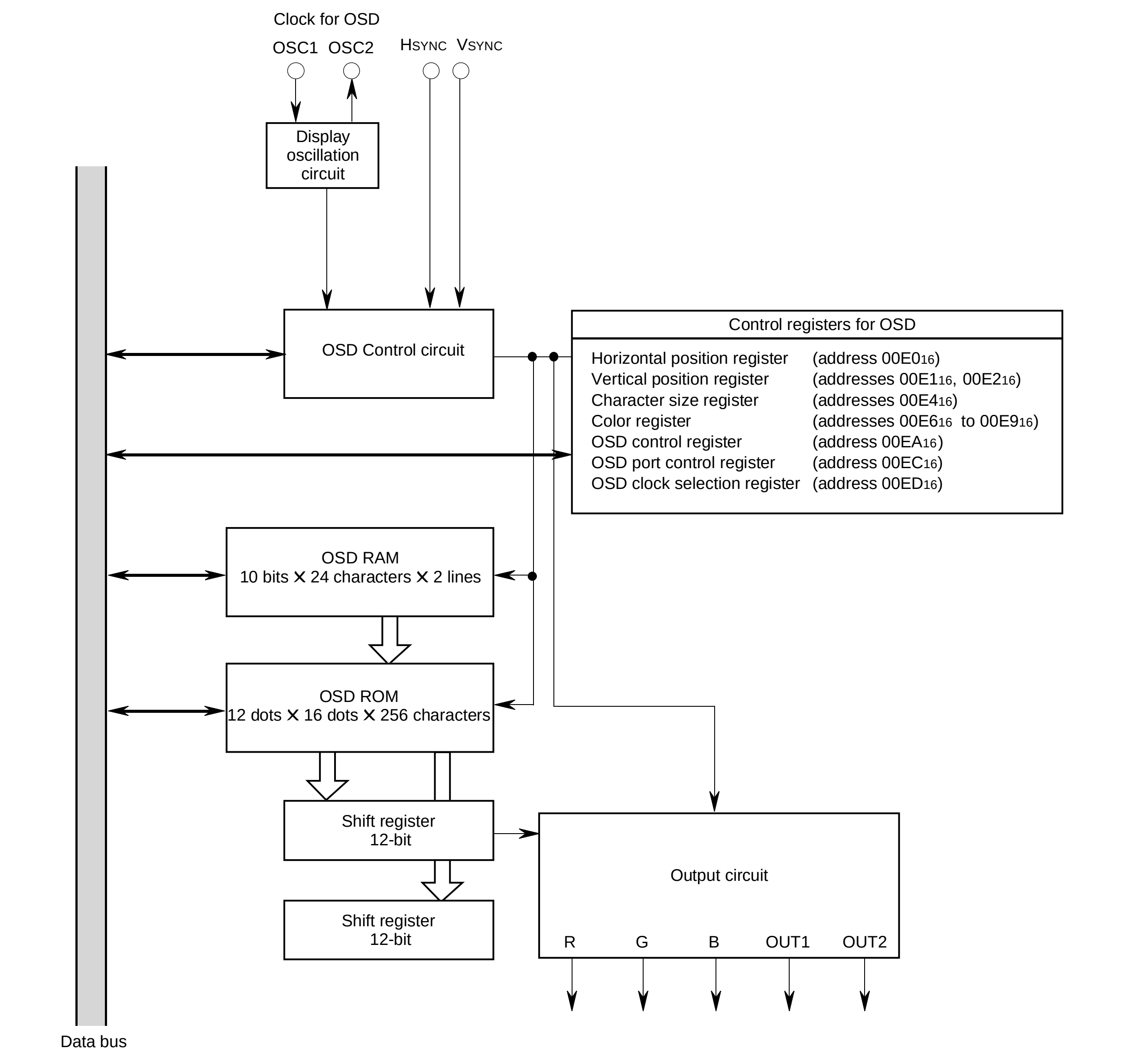


Fig. 8.11.2 Block Diagram of OSD Circuit

OSD Control Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register (CC) [Address $00EA_{16}$]

B	Name	Functions	After reset	R	W
0	All-blocks display control bit (CC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Block 1 display control bit (CC1)	0 : Block 1 display off 1 : Block 1 display on	0	R	W
2	Block 2 display control bit (CC2)	0 : Block 2 display off 1 : Block 2 display on	0	R	W
3 to 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
7	$P1_0$/OUT2 pin switch bit (CC7)	0 : $P1_0$ 1 : OUT2	0	R	W

Note: Display is controlled by logical product (AND) between the all-blocks display control bit and each block control bit.

Fig. 8.11.3 OSD Control Register

8.11.1 Display Position

The display positions of characters are specified in units called "blocks." There are 2 blocks : blocks 1 and 2. Up to 24 characters can be displayed in each block (refer to "8.11.3 Memory for OSD").
The display position of each block can be set in both horizontal and vertical directions by software.
The display start position in the horizontal direction can be selected for all blocks from 64-step display positions in units of 4Tc (Tc = OSD oscillation cycle).
The display start position in the vertical direction for each block can be selected from 128-step display positions in units of 4 scanning lines.

Blocks are displayed in conformance with the following rules:
• Block 2 is displayed after the display of block 1 is completed (Figure 8.11.4 (a)).
• When the display position of block 1 is overlapped with that of block 2 (Figure 8.11.4 (b)), block 1 is displayed in front.
• When another block display position appears while one block is displayed (Figure 8.11.4 (c)),only block 1 is displayed. Similarly, when multiline display, block 1 is displayed after the display of block 2 is completed.

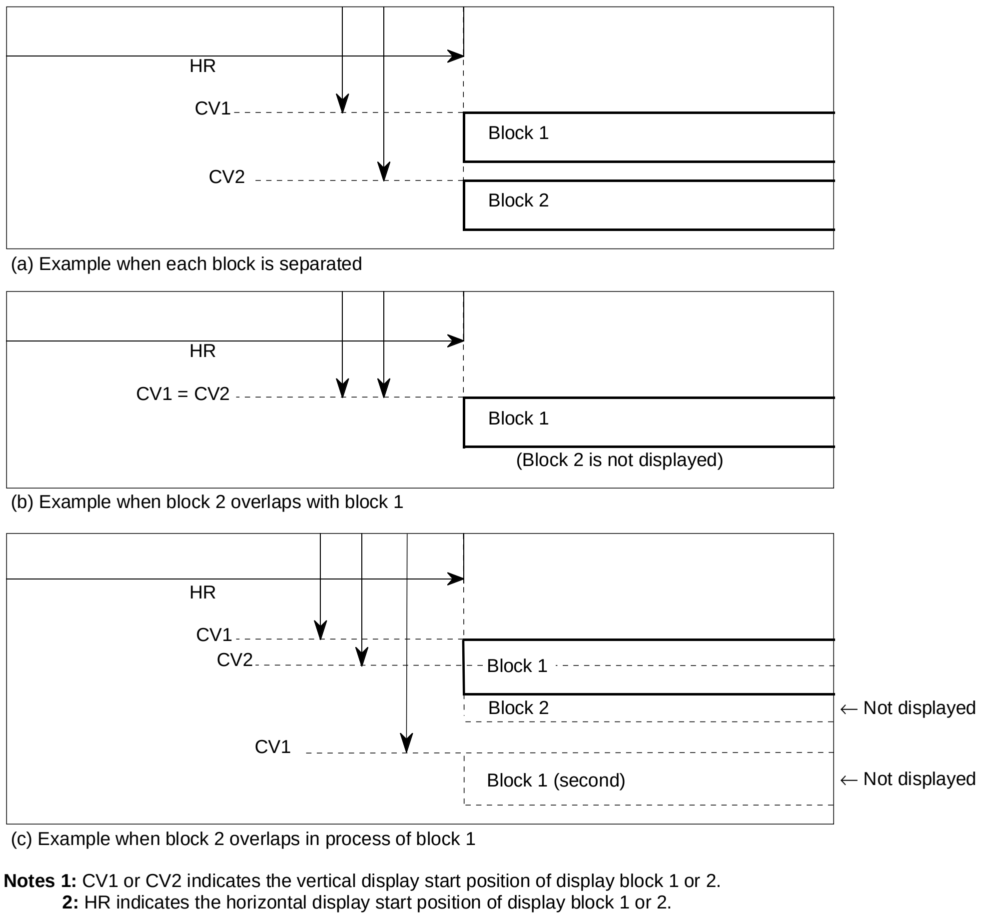
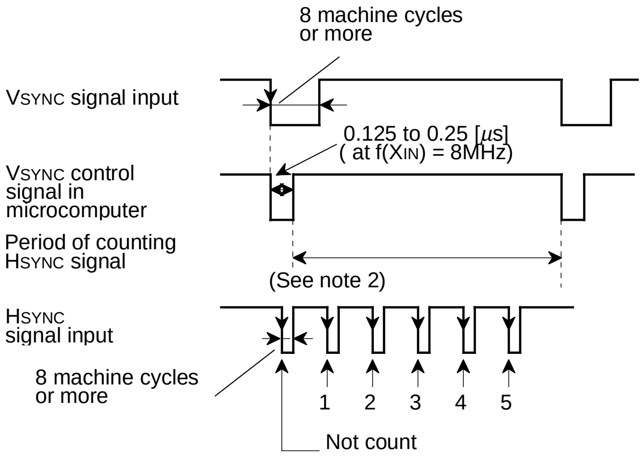


Fig. 8.11.4 Display Position

The vertical display start position is determined by counting the horizontal sync signal (HSYNC). At this time, when VSYNC and HSYNC are positive polarity (negative polarity), the count starts at the rising edge (falling edge) of HSYNC signal after the fixed cycle of the rising edge (falling edge) of VSYNC signal. So the interval from the rising edge (falling edge) of VSYNC signal to the rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) to avoid jitters. The polarity of HSYNC and VSYNC signals can be select with the OSD port control register (address $00EC_{16}$).



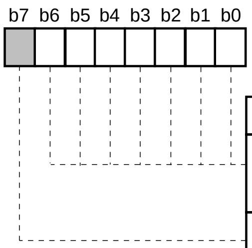
When bits 0 and 1 of the OSD port control register (address $00EC_{16}$) are set to “1” (negative polarity)

Notes 1 : The vertical position is determined by counting falling edge of HSYNC signal after rising edge of VSYNC control signal in the microcomputer.
2 : Do not generate falling edge of HSYNC signal near rising edge of VSYNC control signal in microcomputer to avoid jitter.
3 : The pulse width of VSYNC and HSYNC needs 8 machine cycles or more.

Fig. 8.11.5 Supplement Explanation for Display Position

The vertical display start position for each block can be set in 512 steps (where each step is $1T_H$ (T_H: H_{SYNC} cycle)) as values "00_{16}" to "$7F_{16}$" in vertical position register i (i = 1 and 2) (addresses $00E1_{16}$ and $00E2_{16}$) The vertical position register i is shown in Figure 8.11.6.

Vertical Position Register i



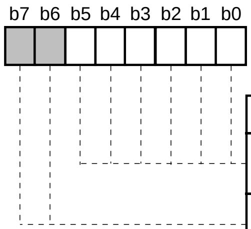
Vertical position register i (CVi) (i = 1 and 2) [Addresses $00E1_{16}$, $00E2_{16}$]

B	Name	Functions	After reset	R	W
0 to 6	Vertical display start positions (CVi : CVi0 to CVi6)	128 steps (00_{16} to $7F_{16}$)	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 8.11.6 Vertical Position Register i

The horizontal display start position is common to all blocks, and can be set in 64 steps (where 1 step is 4T_C, T_C being the OSD oscillation cycle) as values “00_{16}” to “$3F_{16}$” in bits 0 to 5 of the horizontal position register (address $00D1_{16}$). The horizontal position register is shown in Figure 8.11.7.

Horizontal Position Register



Horizontal position register (HR) [Address $00E0_{16}$]

B	Name	Functions	After reset	R	W
0 to 5	Horizontal display start positions (HR0 to HR5)	64 steps (00_{16} to $3F_{16}$)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When thses bits are read out, the values are “0.”		0	R	—

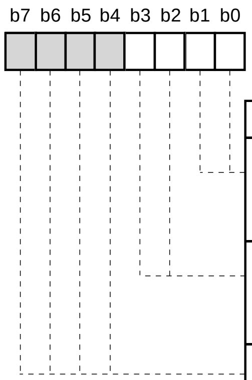
Fig. 8.11.7 Horizontal Position Register

8.11.2 Character Size

The size of characters to be displayed can be from 3 sizes for each block. Use the character size register (address $00E4_{16}$) to set a character size. The character size of block 1 can be specified by using bits 0 and 1 of the character size register; the character size of block 2 can be specified by using bits 2 and 3. Figure 8.11.8 shows the character size register.

The character size can be selected from 3 sizes: minimum size, medium size and large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the oscillating cycle for display (T_C) in the width (horizontal) direction. The minimum size consists of [1 scanning line] × [1T_C]; the medium size consists of [2 scanning lines] × [2T_C]; and the large size consists of [3 scanning lines] × [3T_C]. Table 8.11.2 shows the relation between the set values in the character size register and the character sizes.

Character Size Register



Character size register (CS) [Address $00E4_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Character size of block 1 selection bits (CS10, CS11)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
2,3	Character size of block 2selection bits (CS20,CS21)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 8.11.8 Character Size Register

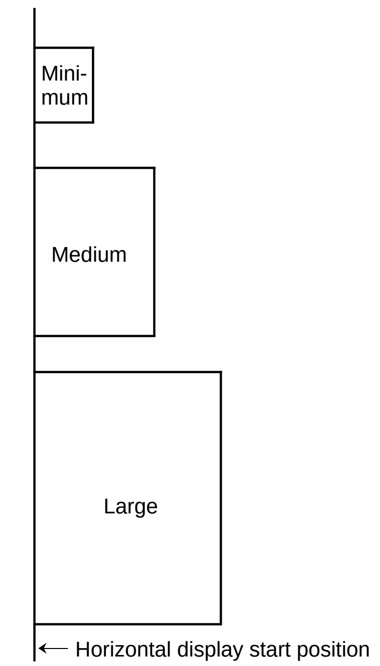


Fig. 8.11.9 Display Start Position of Each Character Size (Horizontal Direction)

Table. 8.11.2 Relation between Set Values in Character Size Register and Character Sizes

Set values of character size register		Character size	Width (horizontal) direction TC: oscillating cycle for display	Height (vertical) direction scanning lines
CSi1	CSi0			
0	0	Minimum	1 TC	1
0	1	Medium	2 TC	2
1	0	Large	3 TC	3
1	1	This is not available		

Notes 1: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 8.11.9).
2: i indicates 1 or 2.

8.11.3 Clock for OSD

The following 2 types of clocks can be selected for OSD display.

- Main clock supplied from X_{IN} pin
- Main clock supplied from X_{IN} pin divided by I.5
- Clock from the ceramic resonator or the LC or oscillator from the pins OSC1 and OSC2
- Clock from the ceramic resonator or the quartz-crystal oscillator supplied from pins OSC1 and OSC2.

The OSD clock for each block can be selected by the OSD clock selection register (address $00ED_{16}$).

When selecting the main clock, set the oscillation frequency to 8 MHz.

OSD Clock Selection Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

OSD clock selection register (CK) [Address $00ED_{16}$]

B	Name	Functions				After reset	R	W
0, 1	OSD clock selection bits (CK0,CK1)	b1	b0	Functions		0	R	W
		0	0	The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.				
		0	1	Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports $P3_3$ and $P3_4$ respectively.	OSD oscillation frequency = $f(X_{IN})$			
		1	0		OSD oscillation frequency = $f(X_{IN})/1.5$			
		1	1	The clock for OSD is supplied by connecting the following across the pins OSC1 and OSC2. • a ceramic resonator only for OSD • a quartz-crystal oscillator only for OSD and a feedback resistor (See note)				
2 to 7	Fix these bits to “0.”					0	R	W

Note: It is necessary to connect other ceramic resonator or quartz-crystal oscillator for OSD across the pINs X_{IN} and X_{OUT}.

Fig. 8.11.10 OSD clock selection Circuit

8.11.4 Memory for OSD

There are 2 types of memory for OSD: OSD ROM (addresses 10000_{16} to $11FFF_{16}$) used to store character dot data and OSD RAM (addresses 0600_{16} to $06B7_{16}$) used to specify the characters and colors to be displayed.

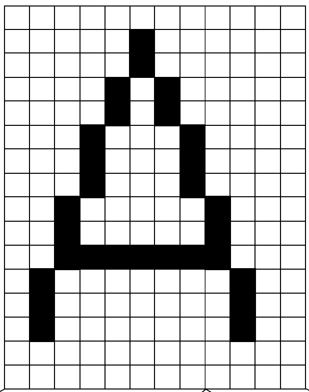
(1) OSD ROM (addresses 10000_{16} to $11FFF_{16}$)

The dot pattern data for OSD characters is stored in the OSD ROM. To specify the kinds of character font, it is necessary to write the character code (Table 8.11.3) into the OSD RAM.

The OSD ROM has a capacity of 8K bytes. Since 32 bytes are required for 1 character data, the ROM can stores up to 256 kinds of characters.

The OSD ROM space is broadly divided into 2 areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 10000_{16} to $107FF_{16}$ and 11000_{16} to $117FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 10800_{16} to $10FFF_{16}$ and 11800_{16} to $11FFF_{16}$ (refer to Figure 8.11.11). Note however that the high-order 4 bits in the data to be written to addresses 10800_{16} to $10FFF_{16}$ and 11800_{16} to $11FFF_{16}$ must be set to “1” (by writing data “FX_{16}”).

Data of the character font is specified shown in Figure 8.11.11.



Left side (10XX0₁₆ or 11XX0₁₆ to 10XXF₁₆ or 11XXF₁₆):

Address	b7							b0
$10XX0_{16}$ or $11XX0_{16}$	0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	0
	0	0	0	0	0	1	0	0
	0	0	0	0	1	0	1	0
	0	0	0	0	1	0	1	0
	0	0	0	1	0	0	0	1
	0	0	0	1	0	0	0	1
	0	0	0	1	0	0	0	1
	0	0	1	0	0	0	0	0
	0	0	1	0	0	0	0	0
	0	0	1	1	1	1	1	1
	0	1	0	0	0	0	0	0
	0	1	0	0	0	0	0	0
	0	1	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
$10XXF_{16}$ or $11XXF_{16}$	0	0	0	0	0	0	0	0

Right side:

Address	b7				b3			b0
$10XX0_{16}$ $+800_{16}$ or $11XX0_{16}$ $+800_{16}$	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	1	0	0	0
	1	1	1	1	1	0	0	0
	1	1	1	1	1	0	0	0
	1	1	1	1	0	1	0	0
	1	1	1	1	0	1	0	0
	1	1	1	1	0	1	0	0
	1	1	1	1	0	0	0	0
$10XXF_{16}$ $+800_{16}$ or $11XXF_{16}$ $+800_{16}$	1	1	1	1	0	0	0	0

Fig. 8.11.11 Character Font Data Storing Address

Table 8.11.3 Character Code List (Partially Abbreviated)

Character code	Character data storage address	
	Left 8 dots lines	Right 4 dots lines
00_{16}	10000_{16} to $1000F_{16}$	10800_{16} to $1080F_{16}$
01_{16}	10010_{16} to $1001F_{16}$	10810_{16} to $1081F_{16}$
02_{16}	10020_{16} to $1002F_{16}$	10820_{16} to $1082F_{16}$
03_{16}	10030_{16} to $1003F_{16}$	10830_{16} to $1083F_{16}$
:	:	:
$7E_{16}$	$107E0_{16}$ to $107EF_{16}$	$10FE0_{16}$ to $10FEF_{16}$
$7F_{16}$	$107F0_{16}$ to $107FF_{16}$	$10FF0_{16}$ to $10FFF_{16}$
80_{16}	11000_{16} to $1100F_{16}$	11800_{16} to $1180F_{16}$
81_{16}	11010_{16} to $1101F_{16}$	11810_{16} to $1181F_{16}$
:	:	:
FD_{16}	$117D0_{16}$ to $117DF_{16}$	$11FD0_{16}$ to $11FDF_{16}$
FE_{16}	$117E0_{16}$ to $117EF_{16}$	$11FE0_{16}$ to $11FEF_{16}$
FF_{16}	$117F0_{16}$ to $117FF_{16}$	$11FF0_{16}$ to $11FFF_{16}$

(2) OSD RAM (addresses 0600_{16} to $06B7_{16}$)

The OSD RAM is allocated at addresses 0600_{16} to $06B7_{16}$, and is divided into a display character code specification part, and color code specification part for each block. Table 8.11.4 shows the contents of the OSD RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0600_{16}, write the color code at 0680_{16}.

The structure of the OSD RAM is shown in Figure 8.11.12.

Table 8.10.4 Contents of OSD RAM

Block	Display Position (from left)	Character Code Specification	Color Specification
Block 1	1st character	0600_{16}	0680_{16}
	2nd character	0601_{16}	0681_{16}
	3rd character : 22nd character	0602_{16} : 0615_{16}	0682_{16} : 0695_{16}
	23rd character	0616_{16}	0696_{16}
	24th character	0617_{16}	0697_{16}
Not used		0618_{16} : $061F_{16}$	0698_{16} : $069F_{16}$
Block 2	1st character	0620_{16}	$06A0_{16}$
	2nd character	0621_{16}	$06A1_{16}$
	3rd character : 22nd character	0622_{16} : 0635_{16}	$06A2_{16}$: $06B5_{16}$
	23rd character	0636_{16}	$06B6_{16}$
	24th character	0637_{16}	$06B7_{16}$

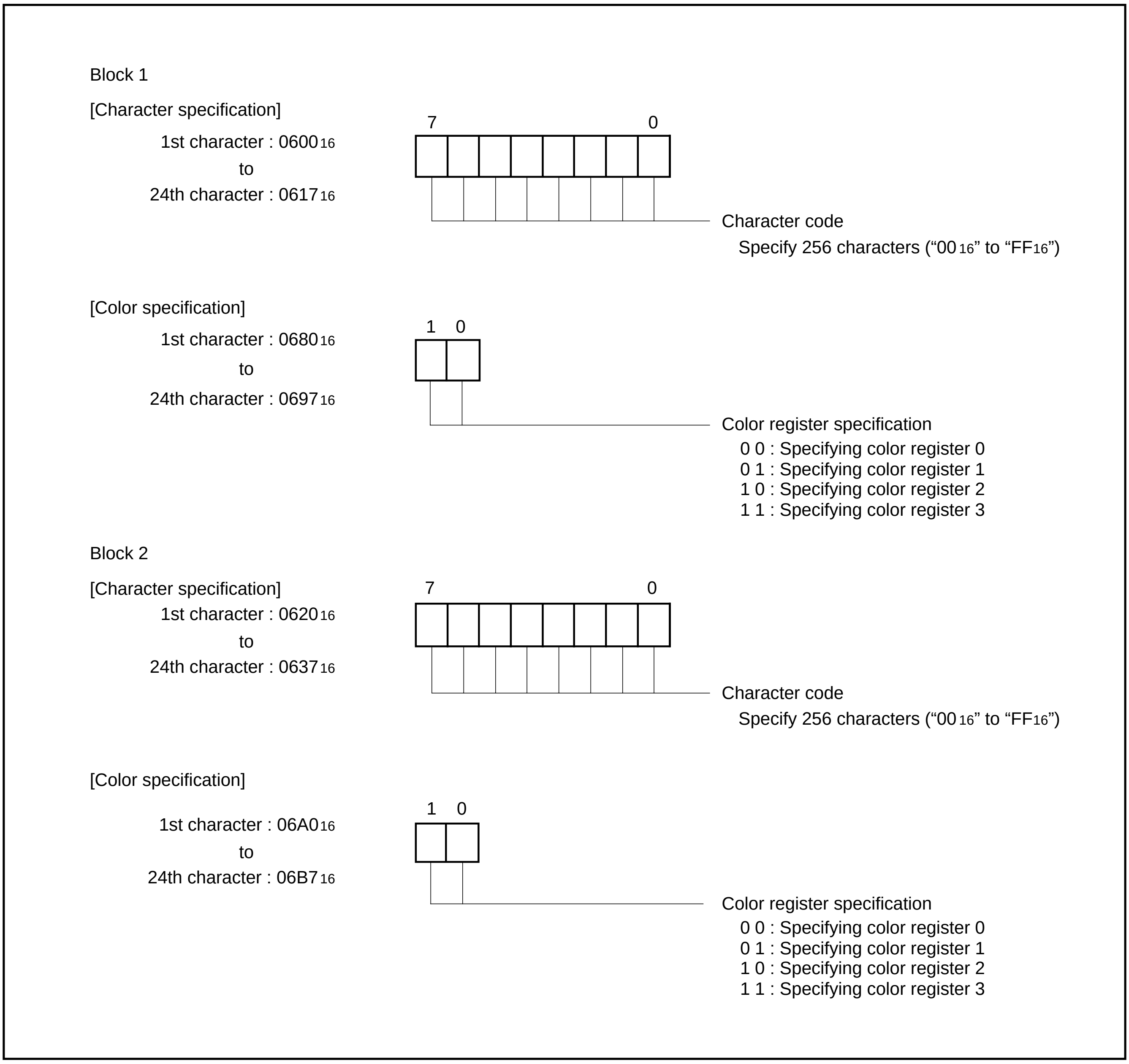


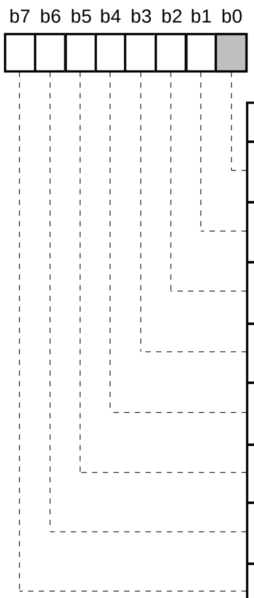
Fig. 8.11.12 Bit structure of OSD RAM

8.11.5 Color Register

The color of a displayed character can be specified by setting the color to one of the 4 registers (CO0 to CO3: addresses $00E6_{16}$ to $00E9_{16}$) and then specifying that color register with the OSD RAM. There are 3 color outputs; R, G and B. By using a combination of these outputs, it is possible to set 8 colors. However, since only 4 color registers are available, up to 4 colors can be disabled at one time.

R, G and B outputs are set by using bits 1 to 3 in the color register. Bit 5 is used to specify whether a character output or blank output. Bits 4, 6 and 7 are used to specify character background color. Figure 8.11.12 shows the color register.

Color Register i



Color register i (COi) (i = 0 to 3) [Addresses $00E6_{16}$ to $00E9_{16}$]

B	Name	Functions	After reset	R	W
0	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
1	B signal output selection bit (COi1)	0: No character is output 1: Character is output	0	R	W
2	G signal output selection bit (COi2)	0: No character is output 1: Character is output	0	R	W
3	R signal output selection bit (COi3)	0: No character is output 1: Character is output	0	R	W
4	B signal output (background) selection bit (COi4) (See note 1)	0: No background color is output 1: Background color is output	0	R	W
5	OUT1 signal output control bit (COi5) (See notes 1, 2)	0: Character is output 1: Blank is output	0	R	W
6	G signal output (background) selection bit (COi6) (See note 1)	0: No background color is output 1: Background color is output	0	R	W
7	R signal output (background) selection bit (COi7) (See note 2)	0: No background color is output 1: Background color is output	0	R	W

Notes 1: When bit 5 ="0" and bit 4 = "1," there is output same as a character or border output from pin OUT1.
Do not set bit 5 = "0" and bit 4 = "0."
2: When only bit 7 ="1" and bit 5 "0," there is output from pin OUT2.

Fig. 8.11.13 Color Register i

Table 8.11.5 Display Example of Character Background Coloring (When Green Is Set for a Character and Blue Is Set for Background Color)

Border selection register	Color register i							G output	B output	OUT1 output	Character output	OUT2 output
MD_0	COi7	COi6	COi5	COi4	COi3	COi2	COi1					
0	0	×	0	1 (Note 1)	0	1	0	A	No output	Same output as character A	Green Video signal and character color (green) are not mixed.	No output (See note 2)
0	1	×	0	1	0	1	0	A	No output	Same output as character A	Green Video signal and character color (green) are not mixed.	Blank output
0	0	0	1	0	0	1	0	A	No output	Blank output	Green TV image of character background is not displayed.	No output (See note 2)
0	0	0	1	1	0	1	0	A	Background	Blank output	Green Blue TV image of character background is not displayed.	No output (See note 2)
1	×	×	0	1	0	1	0	A	No output	Border output (Black)	Border output (Black) Green Video signal and character color (green) are not mixed.	No output (See note 2)
1	0	0	1	0	0	1	0	A	No output	Blank output	Green Black TV image of character background is not displayed.	No output (See note 2)
1	0	0	1	1	0	1	0	A	Background color – border	Blank output	Border output (Black) Green Blue TV image of character background is not displayed.	No output (See note 2)

Notes 1 : When COi5 = "0" and COi4 = "1," there is output same as a character or border output from the OUT1 pin.
Do not set COi5 = "0" and COi4 = "0."
2 : When only COi7 = "1" and COi5 = "0," there is output from pin OUT2.
3 : The portion "A" in which character dots are displayed is not mixed with any TV video signal.
4 : The wavy-lined arrows in the Table denote video signals.
5 : i indicates 0 to 3, × indicates 0 or 1

8.11.6 Border

An border of 1 clock (1 dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT1 pin. In this case, set bit 5 of a color register to "0" (character is output).

Border can be specified in units of block by using the border selection register (address $00E5_{16}$). Figure 8.11.14 shows the border selection register. Table 8.11.6 shows the relationship between the values set in the border selection register and the character border function.

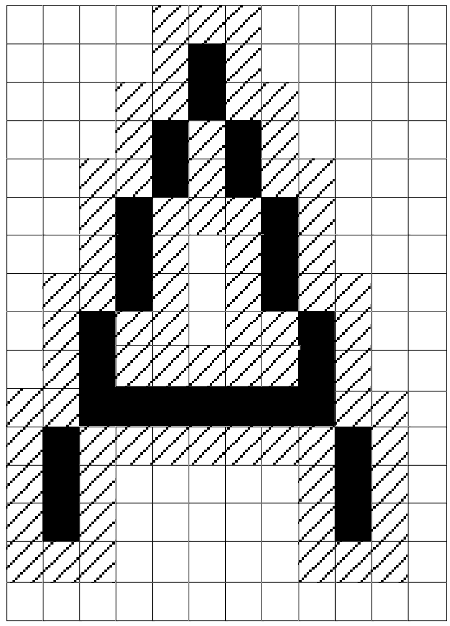


Fig. 8.11.15 Example of Border

Border Selection Register

b7 b6 b5 b4 b3 b2 b1 b0

Border selection register (MD) [Address $00E5_{16}$]

B	Name	Functions	After reset	R	W
0	Block 1 OUT1 output border selection bit (MD10)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
1	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
2	Block 2 OUT1 output border selection bit (MD20)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 8.11.14 Border Selection Register

Table 8.11.6 Relationship between Set Value in Border Selection Register and Character Border Function

Border selection register MDi0	Functions	Example of output
0	Ordinary	R, G, B output OUT1 output
1	Border including character	R, G, B output OUT1 output

Note: i indicates 1or 2

8.11.7 Multiline Display

This microcomputer can ordinarily display 2 lines on the CRT screen by displaying 2 blocks at different vertical positions. In addition, it can display up to 16 lines by using OSD interrupts.

An OSD interrupt request occurs at the point at which that display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

Note: An OSD interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to display off by the display control bit of the OSD control register (address $00EA_{16}$), an OSD interrupt request does not occur (refer to Figure 8.11.16).

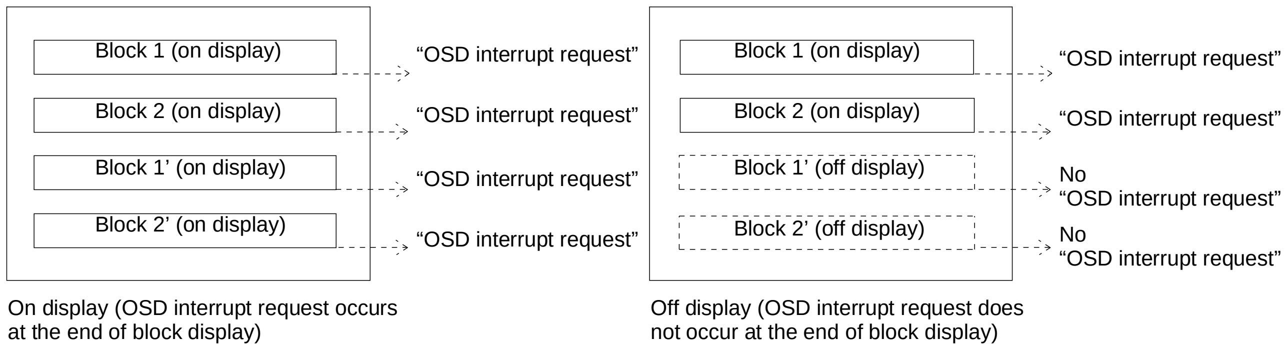


Fig. 8.11.16 Note on Occurence of OSD Interrupt

8.11.8 OSD Output Pin Control

The OSD output pins R, G, B and OUT1 can also function as ports $P5_2$–$P5_5$. Set the corresponding bit of the port P5 direction register (address $00CB_{16}$) to “0” to specify these pins as OSD output pins, or to “1” to specify as the general-purpose port P5.

The OUT2 can also function as port $P1_0$. Set bit 0 of the OSD port control register (address $00EC_{16}$) to “1” (output mode). After that, set bit 7 of the OSD control register to “1” to specify the pin as OSD output pin, or set it to “0” to specify as port $P1_0$.

The input polarity of the HSYNC and VSYNC, and the output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the OSD port control register (address 00EC). Set bits to “0” to specify positive polarity; set it to “1” to specify negative polarity (refer to Figure 8.11.13).

The OSD port control register is shown in Figure 8.11.17.

OSD Port Control Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD port control register (CRTP) [Address $00EC_{16}$]

B	Name	Functions	After reset	R	W
0	HSYNC input polarity switch bit (HSYC)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	VSYNC input polarity switch bit (VSYC)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R/G/B output polarity switch bit (R/G/B)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	OUT2 output polarity switch bit (OUT2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
4	OUT1 output polarity switch bit (OUT1)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	R signal output switch bit (OP5)	0 : R signal output 1 : MUTE signal output	0	R	W
6	G signal output switch bit(OP6)	0 : G signal output 1 : MUTE signal output	0	R	W
7	B signal output switch bit(OP7)	0 : B signal output 1 : MUTE signal output	0	R	W

Fig. 8.11.17 OSD Port Control Register

8.11.9 Raster Coloring Function

An entire screen (raster) can be colored by setting CRT port control register. Since each of the R, G and B pins can be switched to raster coloring output, 8 raster colors can be obtained.

When the character color/character background color overlaps with the raster color, the color (R, G, B, OUT1, OUT2), specified for the character color/character background color, takes priority over the raster color. This ensures that character color/character background color is not mixed with the raster color.

An example of raster coloring is shown in Figure 8.11.18.

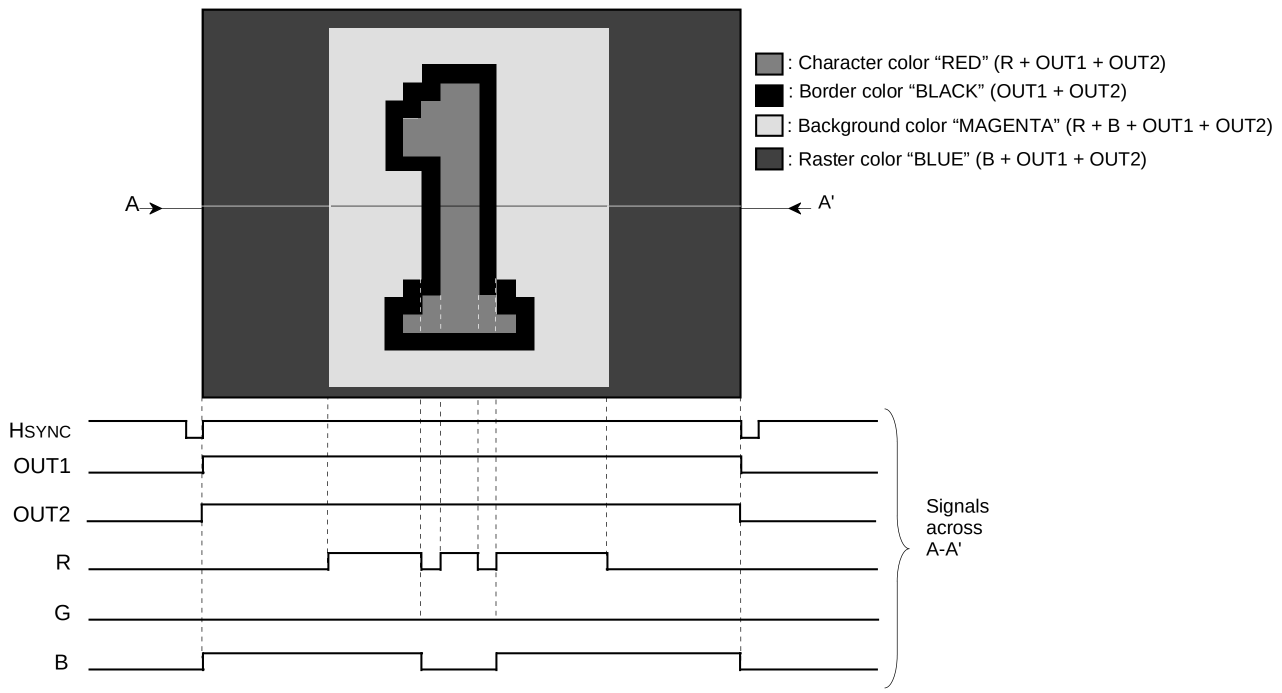


Fig. 8.11.18 Example of Raster Coloring

8.12 SOFTWARE RUNAWAY DETECT FUNCTION

This microcomputer has a function to decode undefined instructions to detect a software runaway.

When an undefined op-code is input to the CPU as an instruction code during operation, the following processing is done.

① The CPU generates an undefined instruction decoding signal.

② The device is internally reset due to the undefined instruction decoding signal.

③ As a result of internal reset, the same reset processing as in the case of ordinary reset operation is done, and the program restarts from the reset vector.

Note, however, that the software runaway detecting function cannot be disabled.

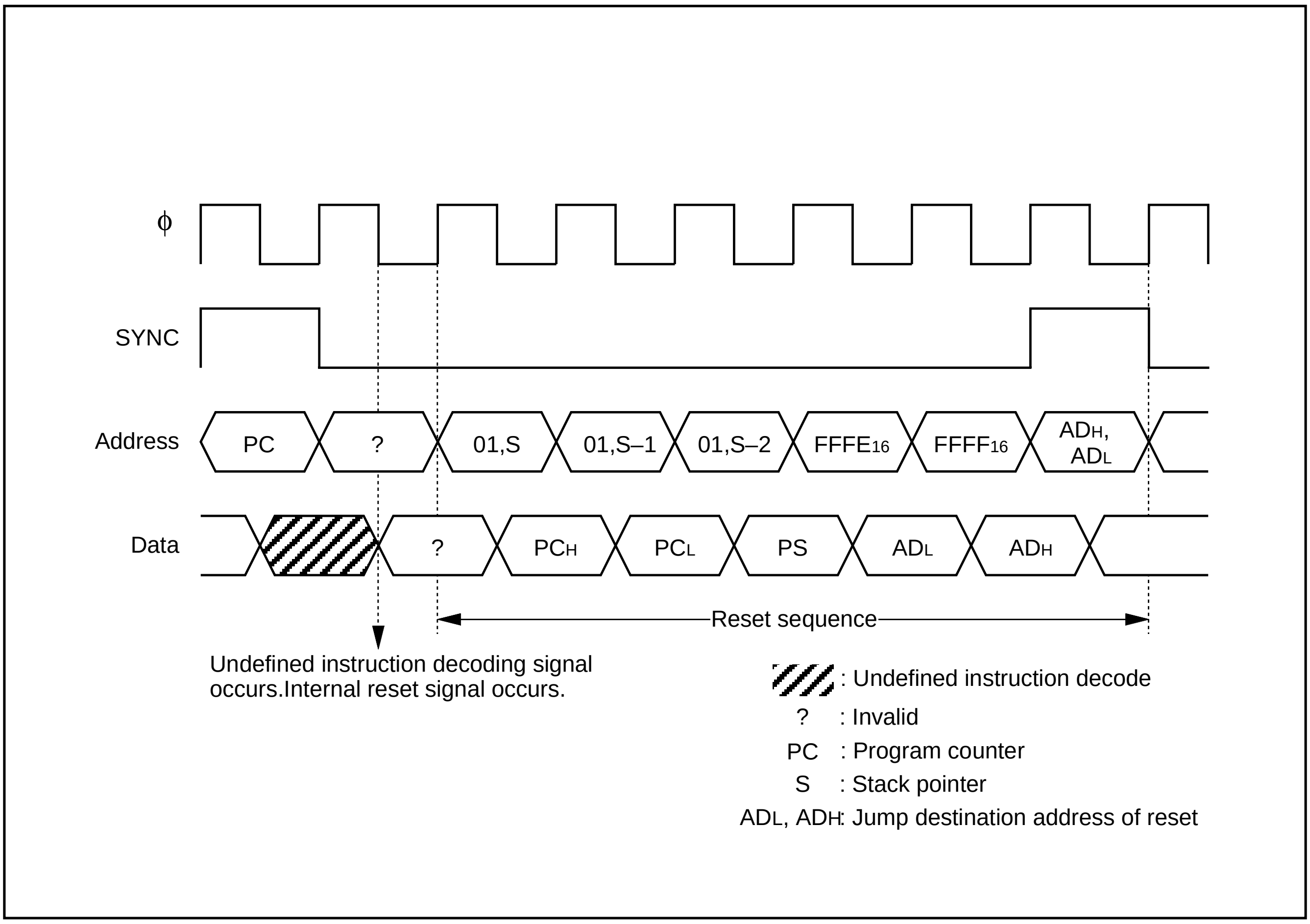


Fig. 8.12.1 Sequence at Detecting Software Runaway Detection

8.13. RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is 5 V ± 10 %, hold the $\overline{\text{RESET}}$ pin at LOW for 2 µs or more, then return to HIGH. Then, as shown in Figure 8.13.2, reset is released and the program starts from the address formed by using the content of address $FFFF_{16}$ as the high-order address and the content of the address $FFFE_{16}$ as the low-order address. The internal states of the microcomputer at reset are shown in Figures 8.2.3 to 8.2.6.
An example of the reset circuit is shown in Figure 8.13.1.
The reset input voltage must be kept 0.6 V or less until the power source voltage surpasses 4.5 V.

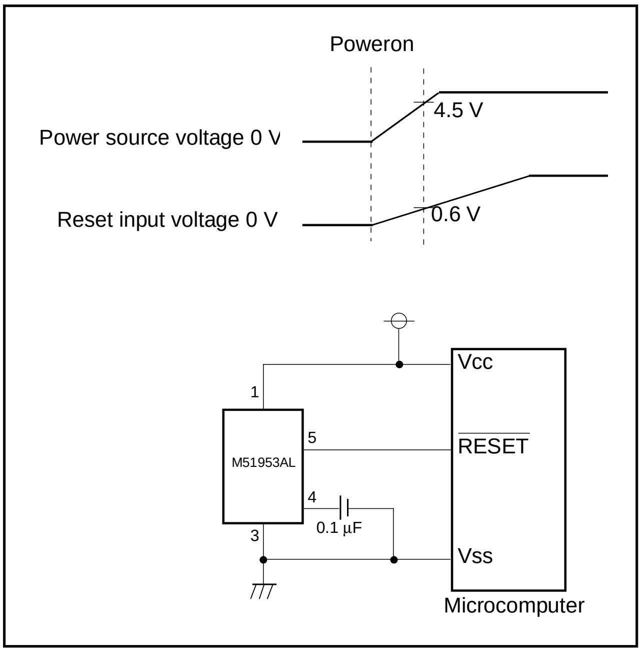
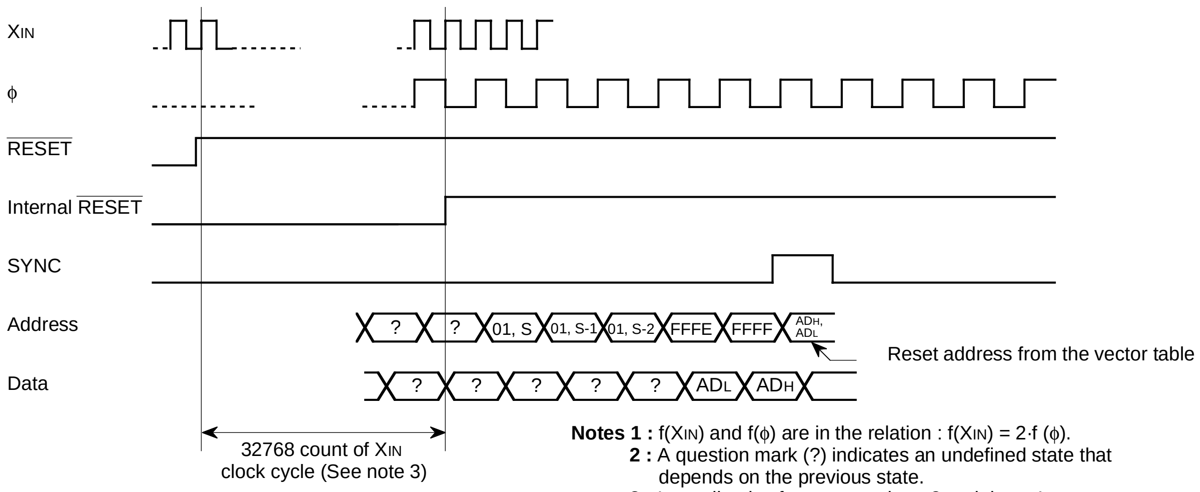


Fig. 8.13.1 Example of Reset Circuit



Notes 1 : f(XIN) and f(φ) are in the relation : f(XIN) = 2·f (φ).
2 : A question mark (?) indicates an undefined state that depends on the previous state.
3 : Immediately after a reset, timer 3 and timer 4 are connected by hardware. At this time, "FF_{16}" is set in timer 3 and "07_{16}" is set to timer 4. Timer 3 counts down with f(XIN)/16, and reset state is released by the timer 4 overflow signal.

Fig. 8.13.2 Reset Sequence

8.14 CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 8.13.3. When the STP instruction is executed, the internal clock ϕ stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF_{16}" is set in timer 3 and "07_{16}" is set in the timer 4. Select f(XIN)/16 as the timer 3 count source (set bit 0 of the timer mode register 2 to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction). The oscillator restarts when external interrupt is accepted. However, the internal clock ϕ keeps its HIGH until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.
When the WIT instruction is executed, the internal clock ϕ stops in the HIGH but the oscillator continues running. This wait state is released when an interrupt is accepted (See note). Since the oscillator does not stop, the next instruction can be executed at once.
When returning from the stop or the wait state, to accept an interrupt, set the corresponding interrupt enable bit to "1" before executing the STP or the WIT instructions.

Note: In the wait mode, the following interrupts are invalid.
- VSYNC interrupt
- OSD interrupt
- Timer 2 interrupt using external clock input from TIM2 pin as count source
- Timer 3 interrupt using external clock input from TIM3 pin as count source
- Timer 4 interrupt using f(XIN)/2 as count source
- Timer 1 interrupt using f(XIN)/4096 as count source
- f(XIN)/4096 interrupt
- Multi-master I^2C-BUS interface interrupt

A circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 8.14.1. Use the circuit constants in accordance with the resonator manufacture's recommended values. A circuit example with external clock input is shown in Figure 8.14.2. Input the clock to the XIN pin, and open the XOUT pin.

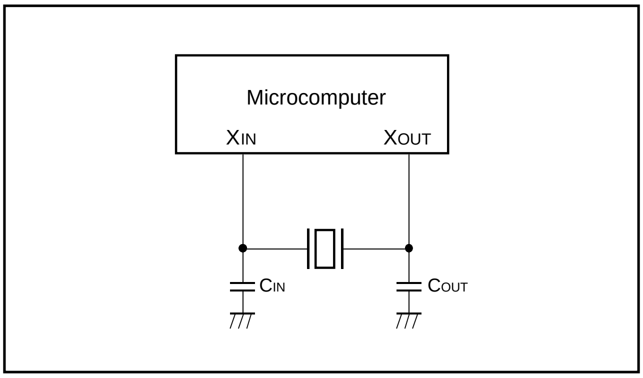


Fig. 8.14.1 Ceramic Resonator Circuit Example

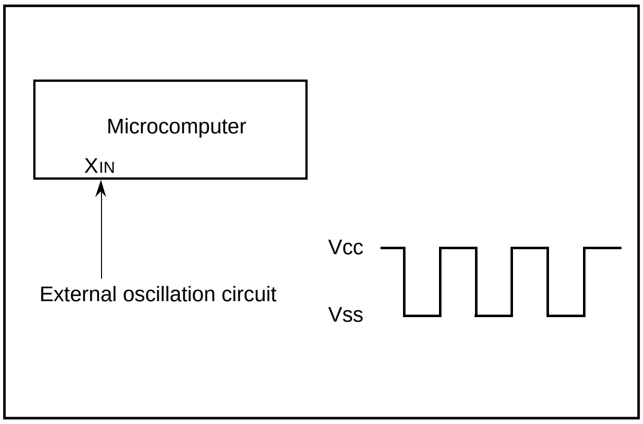


Fig. 8.14.2 External Clock Input Circuit Example

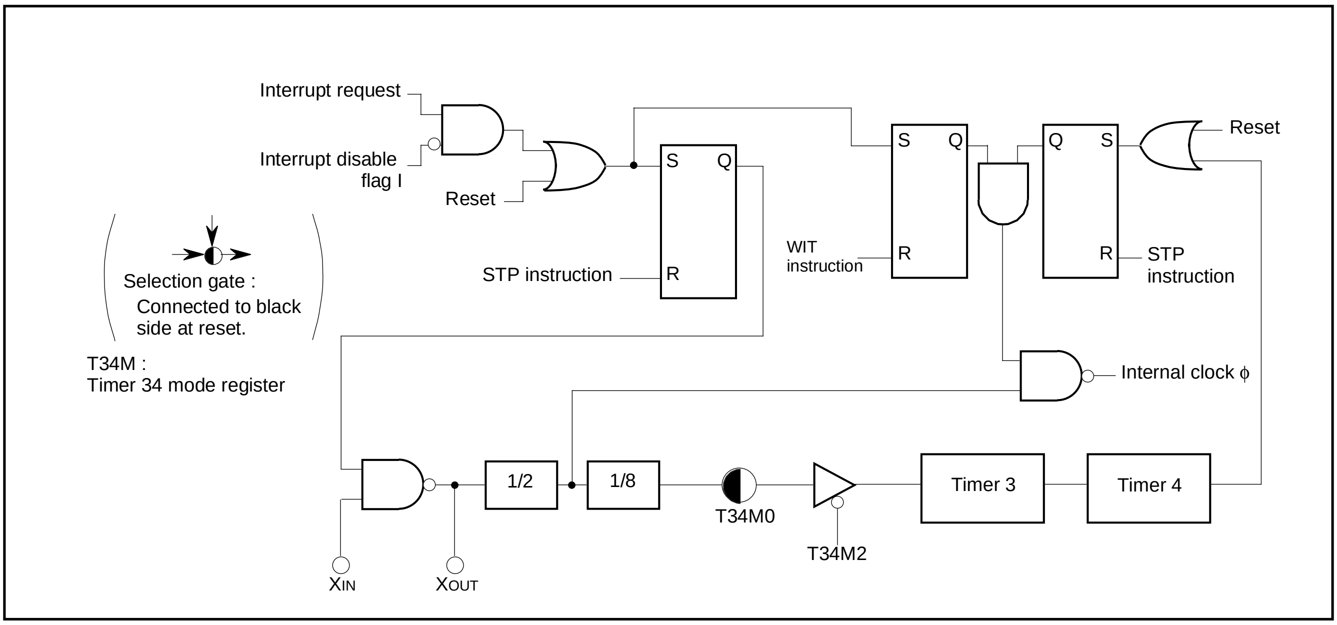


Fig. 8.14.3 Clock Generating Circuit Block Diagram

8.15 DISPLAY OSCILLATION CIRCUIT

The OSD oscillation circuit has a built-in clock oscillation circuits, so that a clock for OSD can be obtained simply by connecting an LC, an RC, a ceramic resonator, or a quartz-crystal oscillator across the pins OSC1 and OSC2. Which of the sub-clock or the OSD oscillation circuit is selected by setting bits 0 and 1 of the OSD clock selection register (address $00ED_{16}$).

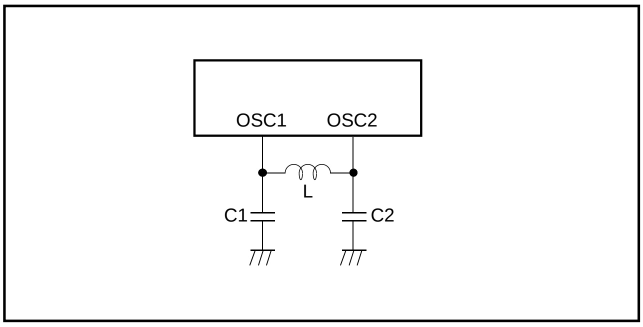
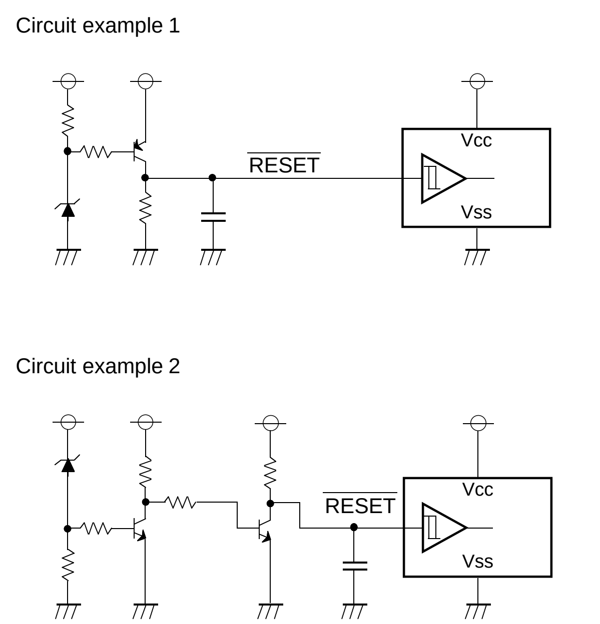


Fig. 8.15.1 Display Oscillation Circuit

8.16 AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the $\overline{\text{RESET}}$ pin.



Note : Make the level change from “L” to “H” at the point at which the power source voltage exceeds the specified voltage.

Fig. 8.16.1 Auto-clear Circuit Example

8.17 ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User’s Manual for details.

8.18 MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Soft- ware> User’s Manual for details.

9. TECHNICAL NOTES

• The divide ratio of the timer is 1/(n+1).

- Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- An NOP instruction is needed immediately after the execution of a PLP instruction.
- In order to avoid noise and latch-up, connect a bypass capacitor (≈ 0.1µF) directly between the V_{CC} pin–V_{SS} pin and the V_{CC} pin–CNV_{SS} pin, using a thick wire.
- [Electric Characteristic Differences Between Mask ROM and One Time PROM Version MCUs]
  There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and One Time PROM version MCUs due to the difference in the manufacturing processes. When manufacturing an application system with the One time PROM version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

10. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage	V_{CC}	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6	V
V_I	Input voltage	CNV_{SS}		–0.3 to 6	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, OSC1, X_{IN}, H_{SYNC}, V_{SYNC}, $\overline{RESET}$		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_2$, R, G, B, OUT1, D-A, X_{OUT}, OSC2		–0.3 to V_{CC} + 0.3	V
I_{OH}	Circuit current	R, G, B, OUT1, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, D-A		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current	R, G, B, OUT1, $P0_0$–$P0_7$, $P1_0$, $P1_5$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_2$, D-A		0 to 2 (Note 2)	mA
I_{OL2}	Circuit current	$P1_1$–$P1_4$		0 to 6 (Note 2)	mA
I_{OL3}	Circuit current	$P2_4$–$P2_7$		0 to 10 (Note 3)	mA
P_d	Power dissipation		T_a = 25 °C	550	mW
T_{opr}	Operating temperature			–10 to 70	°C
T_{stg}	Storage temperature			–40 to 125	°C

11. RECOMMENDED OPERATING CONDITIONS (T_a = –10 °C to 70 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (Note 4), During CPU, CRT operation		4.5	5.0	5.5	V
V_{SS}	Power source voltage		0	0	0	V
V_{IH1}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, S_{IN}, S_{CLK}, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1, TIM2, TIM3, INT1, INT2, INT3	0.8V_{CC}		V_{CC}	V
V_{IH2}	"H" input voltage	SCL1, SCL2, SDA1, SDA2 (When using I^2C-BUS)	0.7V_{CC}		V_{CC}	V
V_{IL1}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$	0		0.4 V_{CC}	V
V_{IL2}	"L" input voltage	SCL1, SCL2, SDA1, SDA2 (When using I^2C-BUS)	0		0.3 V_{CC}	V
V_{IL3}	"L" input voltage	H_{SYNC}, V_{SYNC}, $\overline{RESET}$, TIM2, TIM3, INT1, INT2, INT3, X_{IN}, OSC1, S_{IN}, S_{CLK}	0		0.2 V_{CC}	V
I_{OH}	"H" average output current (Note 1)	R, G, B, OUT1, D-A, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL1}	"L" average output current (Note 2)	R, G, B, OUT1, D-A, $P0_0$–$P0_7$, $P1_0$, $P1_5$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_2$			2	mA
I_{OL2}	"L" average output current (Note 2)	$P1_1$–$P1_4$			6	mA
I_{OL3}	"L" average output current (Note 3)	$P2_4$–$P2_7$			10	mA
f_{CPU}	Oscillation frequency (for CPU operation) (Note 5)	X_{IN}	7.9	8.0	8.1	MHz
f_{CRT}	Oscillation frequency (for CRT display) (Note 5)	OSC1	5.0		8.0	MHz
f_{hs1}	Input frequency	TIM2, TIM3			100	kHz
f_{hs2}	Input frequency	S_{CLK}			1	MHz
f_{hs3}	Input frequency	SCL1, SCL2			400	kHz

Notes 1: The total current that flows out of the IC must be 20 mA (max.).
2: The total input current to IC (I_{OL1} + I_{OL2}) must be 30 mA or less.
3: The total average input current for ports $P2_4$–$P2_7$ to IC must be 20 mA or less.
4: Connect 0.1 µ F or more capacitor externally across the power source pins V_{CC}–V_{SS} so as to reduce power source noise. Also connect 0.1 µ F or more capacitor externally across the pins V_{CC}–CNV_{SS}.
5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.

12. ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit	Test circuit
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	OSD OFF		20	40	mA	1
				OSD ON		30	60		
		Stop mode	V_{CC} = 5.5 V, f(X_{IN}) = 0				300	µA	
V_{OH}	"H" output voltage	R, G, B, OUT1, D-A, $P1_0$–$P1_7$ $P2_0$–$P2_7$, $P3_0$, $P3_1$	V_{CC} = 4.5 V I_{OH} = –0.5 mA		2.4			V	2
V_{OL}	"L" output voltage	R, G, B, OUT1, D-A, $P0_0$–$P0_7$, $P1_0$, $P1_5$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_2$	V_{CC} = 4.5 V I_{OL} = 0.5 mA				0.4	V	
	"L" output voltage	$P1_1$–$P1_4$	V_{CC} = 4.5 V	I_{OL} = 3 mA			0.4		
				I_{OL} = 6 mA			0.6		
	"L" output voltage	$P1_1$–$P1_4$	V_{CC} = 4.5 V I_{OL} = 10.0 mA				3.0		
V_{T+} – V_{T-}	Hysteresis	$\overline{RESET}$	V_{CC} = 5.0 V			0.5	0.7	V	3
	Hysteresis (Note)	HSYNC, VSYNC, TIM2, TIM3, INT1–INT3, SCL1, SCL2, SDA1, SDA2, SIN, SCLK	V_{CC} = 5.0 V			0.5	1.3		
I_{IZH}	"H" input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, HSYNC, VSYNC	V_{CC} = 5.5 V V_I = 5.5 V				5	µA	4
I_{IZL}	"L" input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, HSYNC, VSYNC	V_{CC} = 5.5 V V_I = 0 V				5	µA	
R_{BS}	I²C-BUS·BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V_{CC} = 4.5 V				130	Ω	5

Notes 1: The total current that flows out of the IC must be 20 mA or less.
2: The total input current to IC (I_{OL1} + I_{OL2}) must be 30 mA or less.
3: The total average input current for ports $P2_4$–$P2_7$ to IC must be 20 mA or less.
4: Connect 0.1 µF or more capacitor externally between the power source pins V_{CC}–V_{SS} so as to reduce power source noise.
Also connect 0.1 µF or more capacitor externally between the pins V_{CC}–CNV_{SS}.
5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.
6: $P0_6$, $P0_7$, $P1_5$, $P2_3$, $P2_4$ have hysteresis when used as interrupt input pins or timer input pins. $P1_1$–$P1_4$ have hysteresis when these pins are used as multi-master I²C-BUS interface ports. $P2_0$–$P2_2$ have the hysteresis when used as serial I/O pins.
7: Pin names in each parameter are described as below.
(1) Dedicated pins: dedicated pin names.
(2) Double-/triple-function ports
• Same limits: I/O port name.
• Function other than parts vary from I/O port limits: function pin name.

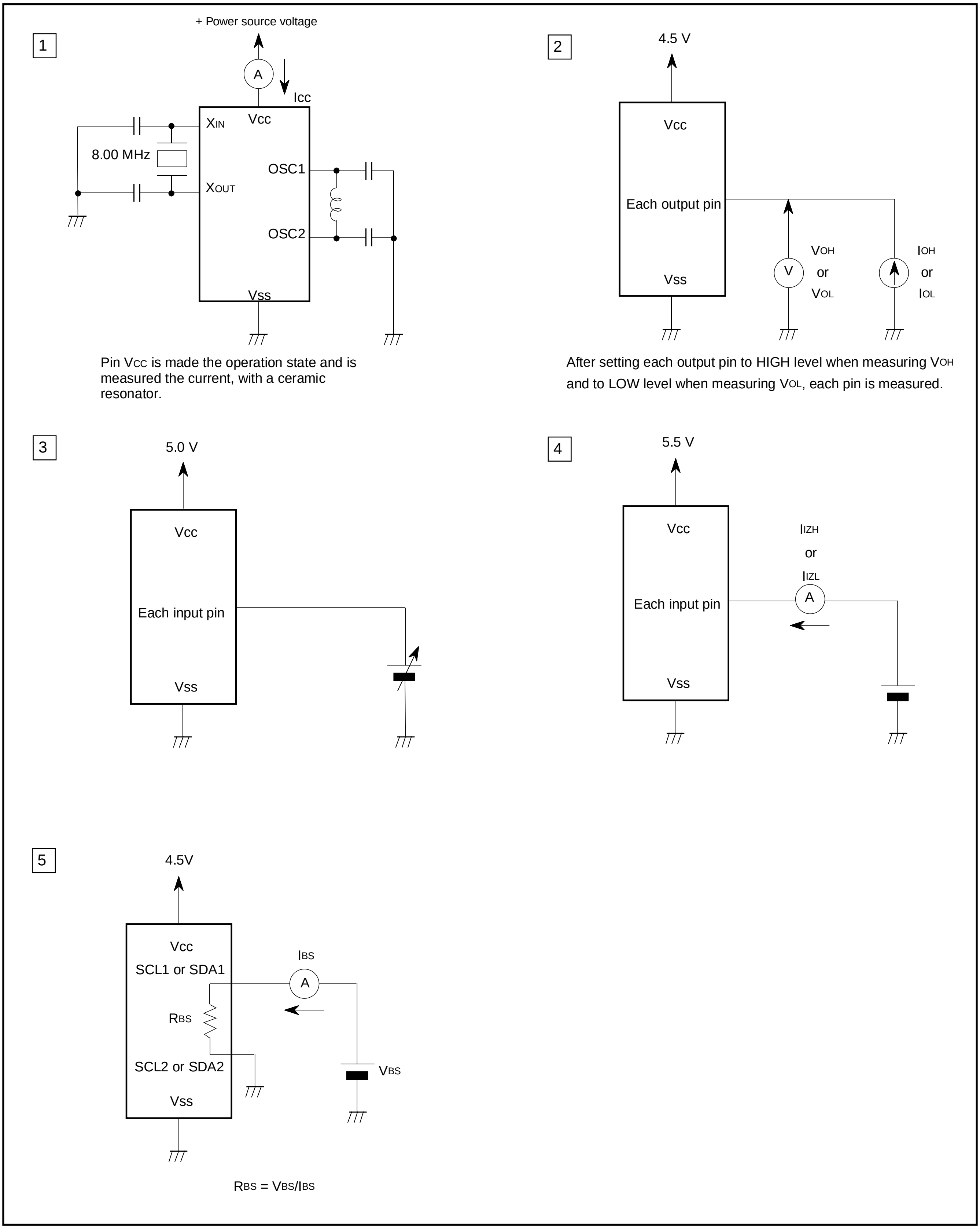


Fig.12.1 Measurement

13. A-D COMPARISON CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = 10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Absolute accuracy		0	±1	±2	LSB

14. D-A CONVERSION CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = 10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Absolute accuracy				2	LSB
tsu	Setting time				3	µs
Ro	Output resistor		1	2.5	4	kΩ

Note: Only M37221EASP/FP have a built-in D-A converter.

15. MULTI-MASTER I^2C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	LOW period of SCL clock	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1C_b	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	HIGH period of SCL clock	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1C_b	300	ns
$t_{SU;DAT}$	Data set-up time	250		100		ns
$t_{SU;STA}$	Set-up time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

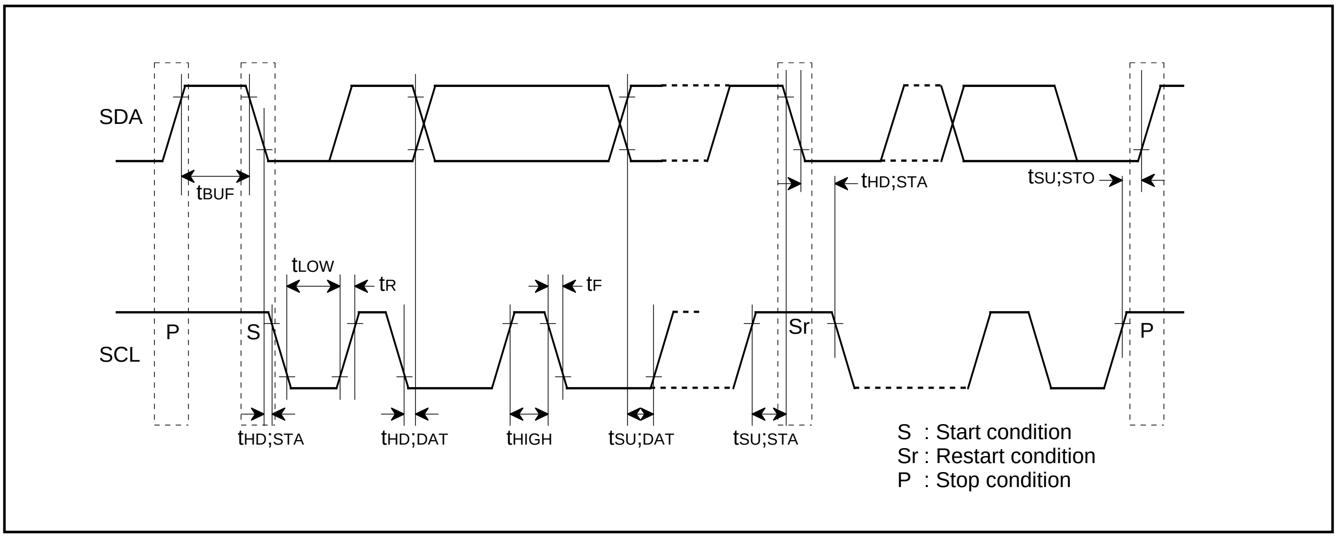


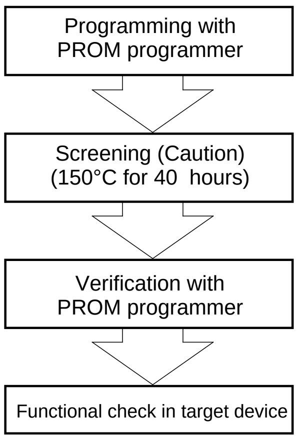
Fig.15.1 Definition Diagram of Timing on Multi-master I^2C-BUS

16. PROM PROGRAMMING METHOD

The built-in PROM of the One Time PROM version (blank) and the built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37221EASP	PCA7408
M37221EAFP	PCA7439

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process nor any following processes. To ensure proper operation after programming, the procedure shown in Figure 16.1 is recommended to verify programming.



Caution : The screening temperature is far higher than the storage temperature. Never expose to 150°C exceeding 100 hours.

Fig. 16.1 Programming and Testing of One Time PROM Version

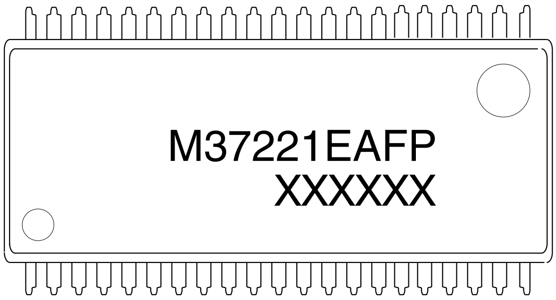
17. DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM product:

- Mask ROM Order Confirmation Form
- Mark Specification Form
- Data to be written to ROM, in EPROM form (32-pin DIP Type 27C101, three identical copies) or FDK

18. ONE TIME PROM VERSION M37221EASP/FP MARKING

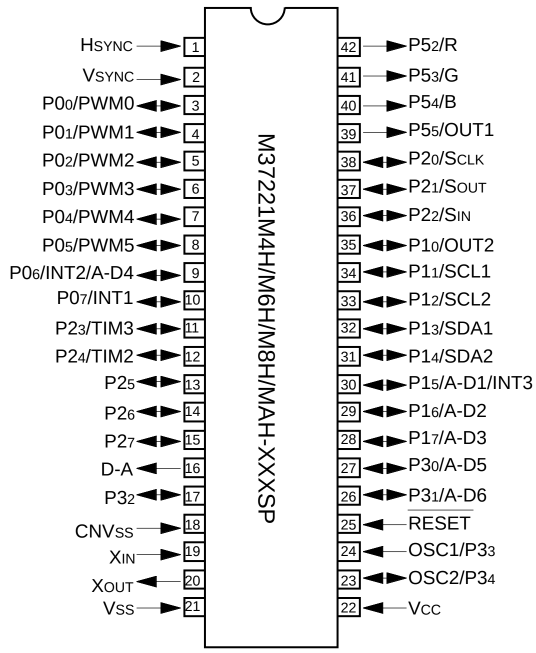
XXXXXX is mitsubishi lot number



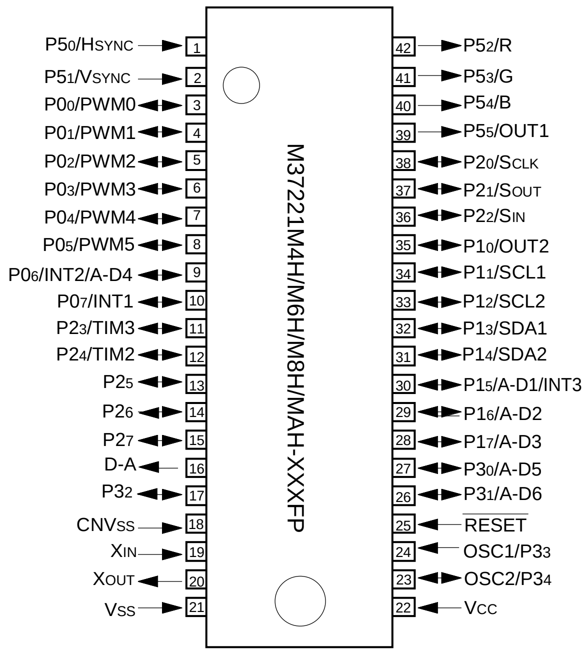
XXXXXX is mitsubishi lot number

19. APPENDIX

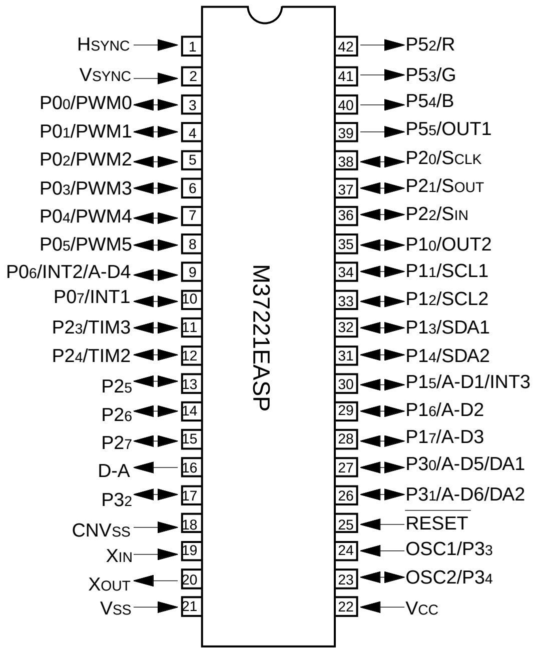
Pin Configuration (TOP VIEW)



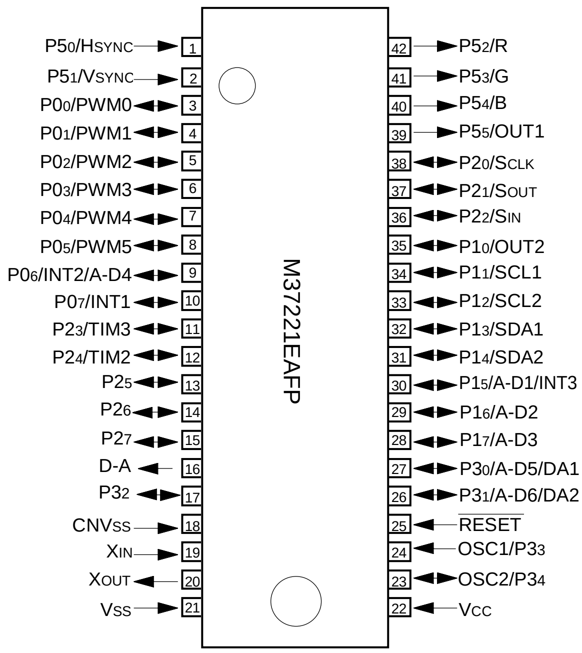
Outline 42P4B



Outline 42P2R-A/E

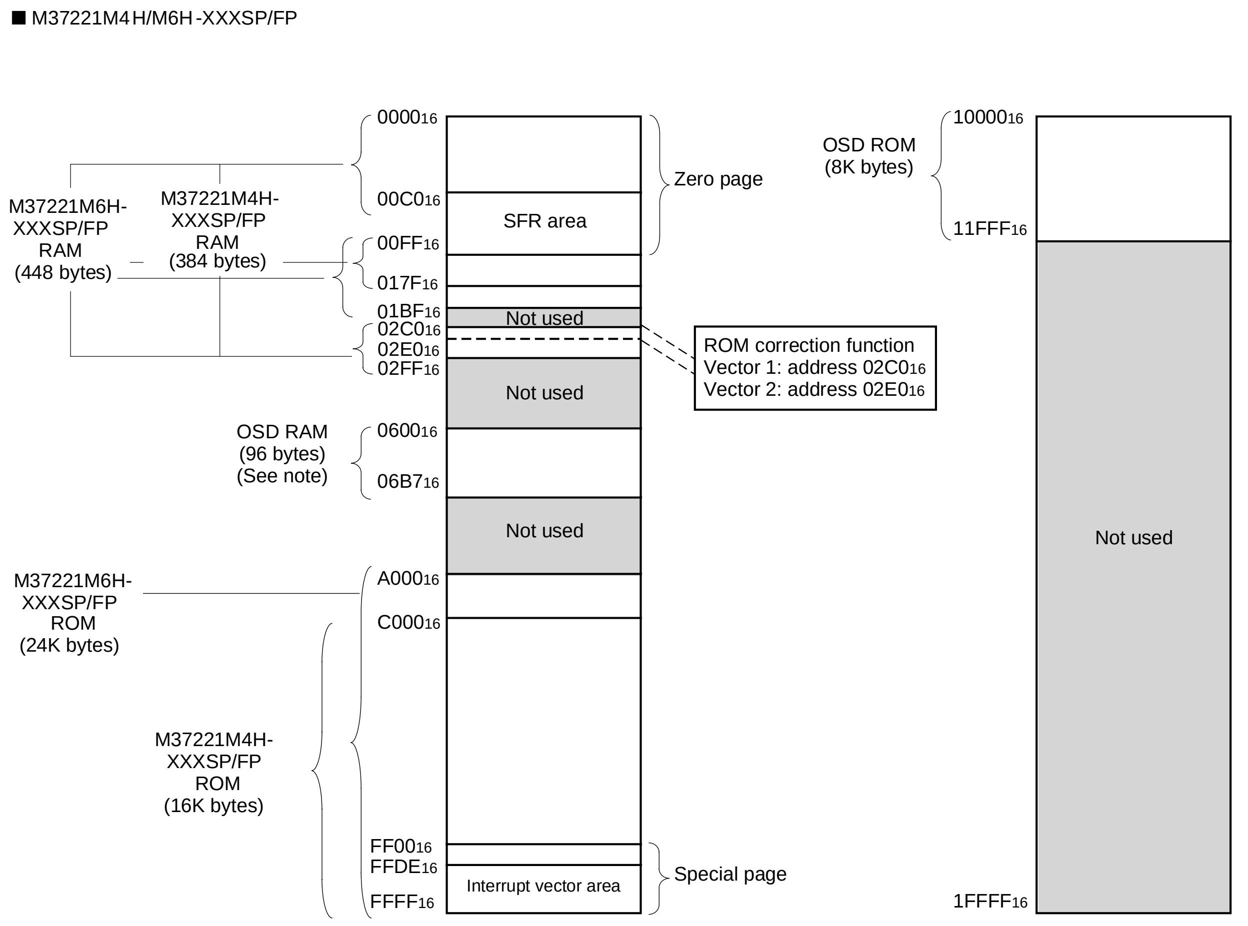


Outline 42P4B



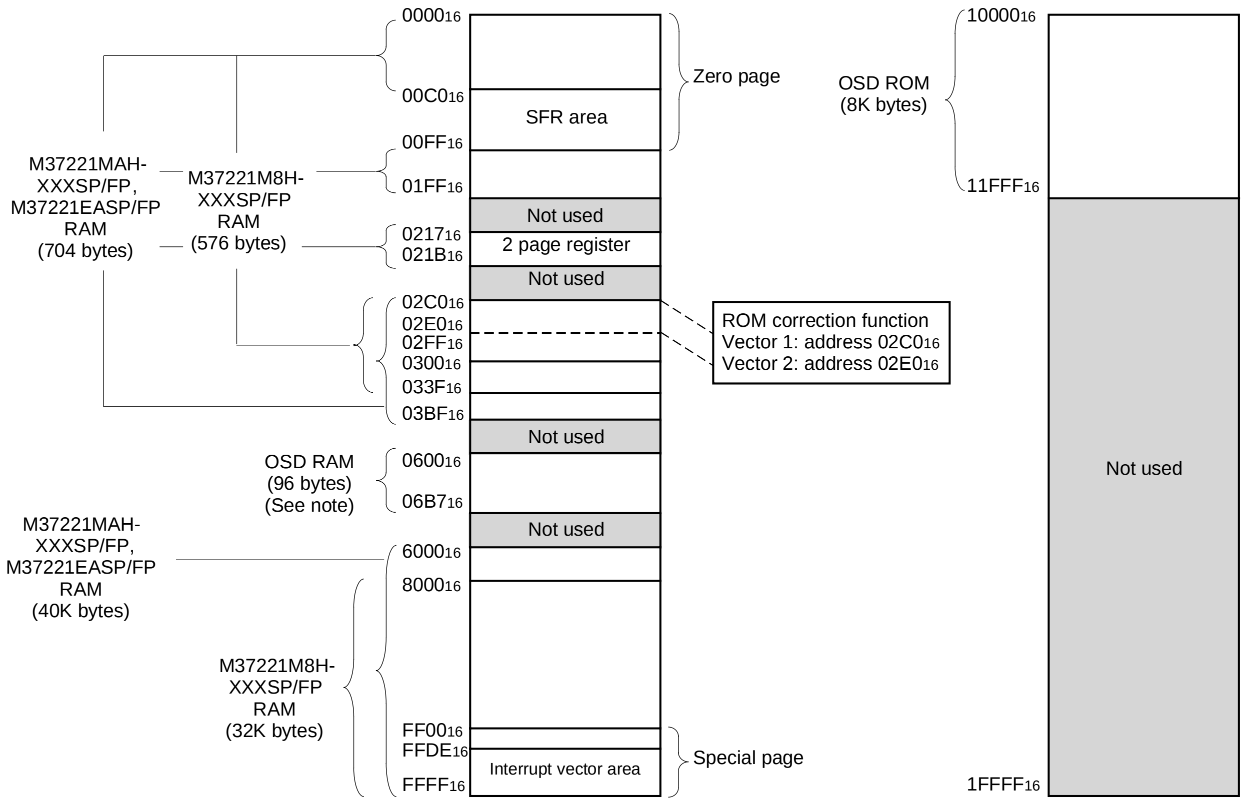
Outline 42P2R-A/E

Memory Map



Note: Refer to Table 8.11.4 OSD RAM.

■ M37221M8H/MAH-XXXSP/FP, M37221EASP/FP



Note: Refer to Table 8.11.4 OSD RAM.

Memory Map of Special Function Register (SFR)

■ SFR area (addresses $C0_{16}$ to DF_{16})

<Bit allocation>

- (blank box) / Name : Function bit
- (shaded box) : No function bit (shown as "—" below)
- 0 (shaded box) : Fix to this bit to "0" (do not write to "1")
- 1 (shaded box) : Fix to this bit to "1" (do not write to "0")

State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$C0_{16}$	Port P0 (P0)									?							
$C1_{16}$	Port P0 direction register (D0)									00_{16}							
$C2_{16}$	Port P1 (P1)									?							
$C3_{16}$	Port P1 direction register (D1)									00_{16}							
$C4_{16}$	Port P2 (P2)									?							
$C5_{16}$	Port P2 direction register (D2)									00_{16}							
$C6_{16}$	Port P3 (P3)	—	—	—						0	0	0	?	?	?	?	?
$C7_{16}$	Port P3 direction register (D3)	—	—	—	—	—				00_{16}							
$C8_{16}$		—	—	—	—	—	—	—	—	?							
$C9_{16}$		—	—	—	—	—	—	—	—	?							
CA_{16}	Port P5 (P5)	—	—					—	—	0	0	?	?	?	?	?	?
CB_{16}	Port P5 direction register (D5)	—	—					—	—	00_{16}							
CC_{16}		—	—	—	—	—	—	—	—	?							
CD_{16}	Port P3 output mode control register (P3S) (Note 1)	—	—	—	—	DA2S	DA1S	P31S	P30S	00_{16}							
CE_{16}	DA-H register (DA-H)									?							
CF_{16}	DA-L register (DA-L)	—	—							0	0	?	?	?	?	?	?
$D0_{16}$	PWM0 register (PWM0)									?							
$D1_{16}$	PWM1 register (PWM1)									?							
$D2_{16}$	PWM2 register (PWM2)									?							
$D3_{16}$	PWM3 register (PWM3)									?							
$D4_{16}$	PWM4 register (PWM4)									?							
$D5_{16}$	PWM output control register 1 (PW)	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00_{16}							
$D6_{16}$	PWM output control register 2 (PN)	—	—	—	PN4	PN3	PN2	—	—	00_{16}							
$D7_{16}$	I^2C data shift register (S0)									?							
$D8_{16}$	I^2C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00_{16}							
$D9_{16}$	I^2C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0	0	0	1	0	0	0	?
DA_{16}	I^2C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ES0	BC2	BC1	BC0	00_{16}							
DB_{16}	I^2C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00_{16}							
DC_{16}	Serial I/O mode register (SM)	—	SM6	SM5	0	SM3	SM2	SM1	SM0	00_{16}							
DD_{16}	Serial I/O regsiter (SIO)									?							
DE_{16}	DA1 conversion register (DA1) (Note 2)	—	0	DA15	DA14	DA13	DA12	DA11	DA10	0	0	?	?	?	?	?	?
DF_{16}	DA2 conversion register (DA2) (Note 2)	—	0	DA25	DA24	DA23	DA22	DA21	DA20	0	0	?	?	?	?	?	?

Note 1: As for M37221M4H/M6H/M8H/MAH-XXXSP/FP, fix bits 2 and 3 to "0."
2: M37221M4H/M6H/M8H/MAH-XXXSP/FP do not have this register. Fix this register to "00_{16}."

■ SFR area (addresses $E0_{16}$ to FF_{16})

<Bit allocation>

- (blank box) : } Function bit
- (Name box) : } Function bit
- (shaded box) : No function bit
- 0 (shaded) : Fix to this bit to "0" (do not write to "1")
- 1 (shaded) : Fix to this bit to "1" (do not write to "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ?

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$E0_{16}$	Horizontal register (HR)			HR5	HR4	HR3	HR2	HR1	HR0	00_{16}							
$E1_{16}$	Vertical register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0	?	?	?	?	?	?	?
$E2_{16}$	Vertical register 2 (CV2)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0	?	?	?	?	?	?	?
$E3_{16}$										?							
$E4_{16}$	Character size register (CS)					CS21	CS20	CS11	CS10	0	0	0	0	?	?	?	?
$E5_{16}$	Border selection register (MD)						MD20		MD10	0	0	0	0	0	?	0	?
$E6_{16}$	Color register 0 (CO0)	CO07	CO06	CO05	CO04	CO03	CO02	CO01		00_{16}							
$E7_{16}$	Color register 1 (CO1)	CO17	CO16	CO15	CO14	CO13	CO12	CO11		00_{16}							
$E8_{16}$	Color register 2 (CO2)	CO27	CO26	CO25	CO24	CO23	CO22	CO21		00_{16}							
$E9_{16}$	Color register 3 (CO3)	CO37	CO36	CO35	CO34	CO33	CO32	CO31		00_{16}							
EA_{16}	OSD control register (CC)	CC7					CC2	CC1	CC0	00_{16}							
EB_{16}										?							
EC_{16}	OSD port control register (CRTP)	OP7	OP6	OP5	OUT1	OUT2	R/G/B	VSYC	HSYC	00_{16}							
ED_{16}	OSD clock selection register (CK)	0	0	0	0	0	0	CK1	CK0	00_{16}							
EE_{16}	A-D control register 1 (AD1)				ADM4		ADM2	ADM1	ADM0	0	0	0	?	0	0	0	0
EF_{16}	A-D control register 2 (AD2)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	00_{16}							
$F0_{16}$	Timer 1 (TM1)									FF_{16}							
$F1_{16}$	Timer 2 (TM2)									07_{16}							
$F2_{16}$	Timer 3 (TM3)									FF_{16}							
$F3_{16}$	Timer 4 (TM4)									07_{16}							
$F4_{16}$	Timer 12 mode register (T12M)			0	T12M4	T12M3	T12M2	T12M1	T12M0	00_{16}							
$F5_{16}$	Timer 34 mode register (T34M)			T34M5	T34M4	T34M3	T34M2	T34M1	T34M0	00_{16}							
$F6_{16}$	PWM5 register (PWM5)									?							
$F7_{16}$										?							
$F8_{16}$										?							
$F9_{16}$	Interrupt input polarity register (RE)	0		RE5	RE4	RE3	0	0		0	0	0	0	0	0	0	?
FA_{16}	Test register (TEST)	00_{16}								00_{16}							
FB_{16}	CPU mode register (CPUM)	1	1	1	1	1	CM2	0	0	1	1	1	1	1	1	0	0
FC_{16}	Interrupt request register 1 (IREQ1)	IT3R	IICR	VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	00_{16}							
FD_{16}	Interrupt request register 2 (IREQ2)	0			MSR		S1R	1T2R	1T1R	00_{16}							
FE_{16}	Interrupt control register 1 (ICON1)	IT3E	IICE	VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	00_{16}							
FF_{16}	Interrupt control register 2 (ICON2)	0	0	0	MSE	0	S1E	1T2E	1T1E	00_{16}							

■ 2 page register area (addresses 217_{16} to $21B_{16}$)

<Bit allocation>

- [ ] : / [Name] : Function bit
- [shaded] : No function bit
- [0] : Fix to this bit to "0" (do not write to "1")
- [1] : Fix to this bit to "1" (do not write to "0")

State immediately after reset>

- [0] : "0" immediately after reset
- [1] : "1" immediately after reset
- [?] : Indeterminate immediately after reset

Address	Register	b7							b0	State immediately after reset (b7–b0)
217_{16}	ROM correction address 1 (high-order)									00_{16}
218_{16}	ROM correction address 1 (low-order)									00_{16}
219_{16}	ROM correction address 2 (high-order)									00_{16}
$21A_{16}$	ROM correction address 2 (low-order)									00_{16}
$21B_{16}$	ROM correction enable register (RCR)					0	0	RCR1	RCR0	00_{16}

Note: Only M37221M4H/M6H/ M8H/MAH-XXXSP/FP and M37221EASP/FP have 2 page register.

Internal State of Processor Status Register and Program Counter at Reset

<Bit allocation>

- [ ] : / [Name] : } Function bit
- [shaded] : No function bit
- [0 shaded] : Fix to this bit to “0” (do not write to “1”)
- [1 shaded] : Fix to this bit to “1” (do not write to “0”)

<State immediately after reset>

- [0] : “0” immediately after reset
- [1] : “1” immediately after reset
- [?] : Indeterminate immediately after reset

Register	Bit allocation b7							b0	State immediately after reset b7							b0
Processor status register (PS)	N	V	T	B	D	I	Z	C	?	?	?	?	?	1	?	?
Program counter (PCH)									Contents of address $FFFF_{16}$							
Program counter (PCL)									Contents of address $FFFE_{16}$							

Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

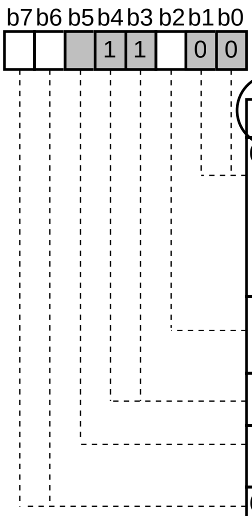
<Example>

CPU Mode Register

Bit position

Bit attributes (Note 2)

Values immediately after reset release (Note 1)



CPU mode register (CPUM) (CM) [Address 00FB16]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } Not available 1 0: 1 1:	0	R	W
2	Stack page selection bit (See note) (CM2)	0: 0 page 1: 1 page	1	R	W
3, 4	Fix these bits to “1.”		1	R	W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is “1.”		1	R	W
6, 7	Clock switch bits (CM6, CM7)	b7 b6 0 0: f(XIN) = 8 MHz 0 1: f(XIN) = 12 MHz 1 0: f(XIN) = 16 MHz 1 1: Do not set	0	R	W

■ : Bit in which nothing is assigned

Notes 1: Values immediately after reset release
0 ••••••••••••••••••“0” after reset release
1 ••••••••••••••••••“1” after reset release
Indeterminate•••Indeterminate after reset release

2: Bit attributes••••••The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R••••••Read
R ••••••Read enabled
– ••••••Read disabled

W••••••Write
W ••••••Write enabled
– ••••••Write disabled
✻ ••••••“0” can be set by software, but “1” cannot be set.

Addresses 00C1$_{16}$, 00C3$_{16}$, 00C5$_{16}$

Port Pi Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (Di) (i=0,1,2) [Addresses 00C1$_{16}$, 00C3$_{16}$, 00C5$_{16}$]

B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port Pi$_0$ input mode 1 : Port Pi$_0$ output mode	0	R	W
1		0 : Port Pi$_1$ input mode 1 : Port Pi$_1$ output mode	0	R	W
2		0 : Port Pi$_2$ input mode 1 : Port Pi$_2$ output mode	0	R	W
3		0 : Port Pi$_3$ input mode 1 : Port Pi$_3$ output mode	0	R	W
4		0 : Port Pi$_4$ input mode 1 : Port Pi$_4$ output mode	0	R	W
5		0 : Port Pi$_5$ input mode 1 : Port Pi$_5$ output mode	0	R	W
6		0 : Port Pi$_6$ input mode 1 : Port Pi$_6$ output mode	0	R	W
7		0 : Port Pi$_7$ input mode 1 : Port Pi$_7$ output mode	0	R	W

Address 00C7$_{16}$

Port P3 Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Port P3 direction register (D3) [Address 00C7$_{16}$]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port P3$_0$ input mode 1 : Port P3$_0$ output mode	0	R	W
1		0 : Port P3$_1$ input mode 1 : Port P3$_1$ output mode	0	R	W
2		0 : Port P3$_2$ input mode 1 : Port P3$_2$ output mode	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		indeterminate	R	—

Address $00CB_{16}$

Port P5 Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Port P5 direction register (D5) [Address $00CB_{16}$]

b	Name	Functions	After reset	R	W
0, 1	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
2	Port $P5_2$ output signal selection bit (P52SEL)	0 : R signal output 1 : Port $P5_2$ output	0	R	W
3	Port $P5_3$ output signal selection bit (P53SEL)	0 : G signal output 1 : Port $P5_3$ output	0	R	W
4	Port $P5_4$ output signal selection bit (P54SEL)	0 : B signal output 1 : Port $P5_4$ output	0	R	W
5	Port $P5_5$ output signal selection bit (P55SEL)	0 : OUT1 signal output 1 : Port $P5_5$ output	0	R	W
6,7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.		Indeterminate	R	—

Address $00CD_{16}$

P3 output mode control register

b7 b6 b5 b4 b3 b2 b1 b0

P3 output mode control register(P3S) [Address $00CD_{16}$]

B	Name	Functions	After reset	R	W
0	$P3_0$ output form selection bit (P30S)	0: CMOS output 1: N-channel open-drain output	0	R	W
1	$P3_1$ output form selection bit (P31S)	0: CMOS output 1: N-channel open-drain output	0	R	W
2	DA1 output enable bit (DA1S)	0: $P3_0$ input/output 1: DA1 output	0	R	W
3	DA2 output enable bit (DA2S)	0: $P3_1$ input/output 1: DA2 output	0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address $00D5_{16}$

PWM Output Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

PWM output control register 1 (PW) [Address $00D5_{16}$]

B	Name	Functions	After reset	R	W
0	DA, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA/PN4 selection bit (PW1)	0 : DA output 1 : PN4 output	0	R	W
2	$P0_0$/PWM0 output selection bit (PW2)	0: $P0_0$ output 1: PWM0 output	0	R	W
3	$P0_1$/PWM1 output selection bit (PW3)	0: $P0_1$ output 1: PWM1 output	0	R	W
4	$P0_2$/PWM2 output selection bit (PW4)	0: $P0_2$ output 1: PWM2 output	0	R	W
5	$P0_3$/PWM3 output selection bit (PW5)	0: $P0_3$ output 1: PWM3 output	0	R	W
6	$P0_4$/PWM4 output selection bit (PW6)	0: $P0_4$ output 1: PWM4 output	0	R	W
7	$P0_5$/PWM5 output selection bit (PW7)	0: $P0_5$ output 1: PWM5 output	0	R	W

Address $00D6_{16}$

PWM Output Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

PWM output control register 2 (PN) [Address $00D6_{16}$]

B	Name	Functions	After reset	R	W
0,1	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
2	DA output polarity selection bit (PN2)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA general-purpose output bit (PN4)	0 : Output LOW 1 : Output HIGH	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address 00D7$_{16}$

I^{2}C Data Shift Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C data shift register (S0) [Address 00D7$_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I^{2}C data shift register after setting the MST bit to “0” (slave mode), keep an interval of 8 machine cycles or more.

Address 00D8$_{16}$

I^{2}C Address Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C address register (S0D) [Address 00D8$_{16}$]

B	Name	Functions	After reset	R	W
0	$\overline{\text{Read}}$/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Address 00D9$_{16}$

I^{2}C Status Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C status register (S1) [Address 00D9$_{16}$]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0 " 1 : Last bit = "1 " (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I^{2}C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave recieve mode 0 1 : Slave transmit mode 1 0 : Master recieve mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannnot be written.

Address 00DA$_{16}$

I^{2}C Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I^{2}C control register (S1D) [Address 00DA$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R	W
3	I^{2}C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit(ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I^{2}C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

Address $00DB_{16}$

I²C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C clock control register (S2) [Address $00DB_{16}$]

B	Name	Functions			After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4–CCR0	Standard clock mode	High speed clock mode	0	R	W
		00 to 02	Setup disabled	Setup disabled			
		03	Setup disabled	333			
		04	Setup disabled	250			
		05	100	400 (See note)			
		06	83.3	166			
		⋮	500/CCR value	1000/CCR value			
		1D	17.2	34.5			
		1E	16.6	33.3			
		1F	16.1	32.3			
		(at φ = 4 MHz, unit : kHz)					
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R	W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R	W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
"0" period : "1" period = 3 : 2
In the other cases, the duty is as below.
"0" period : "1" period = 1 : 1

Address $00DC_{16}$

Serial I/O Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

(b4 = 0)

Serial I/O mode register (SM) [Address $00DC_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(XIN)/4 0 1: f(XIN)/16 1 0: f(XIN)/32 1 1: f(XIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Serial I/O port selection bit (SM3)	0: $P2_0$, $P2_1$ 1: SCLK, SOUT	0	R	W
4	Fix this bit to "0."		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Serial input pin selection bit (SM6)	0: Input signal from SIN pin. 1: Input signal from SOUT pin.	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Addresses 00DE16 and 00DF16

DA conversion register i

b7 b6 b5 b4 b3 b2 b1 b0 (b6 = 0)

DA conversion register i (i=1, 2) (DAi) [Addresses 00DE16, 00DF16]

B	Name	Functions	After reset	R	W
0 to 5	DA conversion selection bit (DAi0 to DAi5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 0/64Vcc 0 0 0 0 0 1 : 1/64Vcc 0 0 0 0 1 0 : 2/64Vcc ⋮ 1 1 1 1 0 1 : 61/64Vcc 1 1 1 1 1 0 : 62/64Vcc 1 1 1 1 1 1 : 63/64Vcc	0	R	W
6	Fix this bit to “0.”		0	R	W
7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Note : When use M37221M4H/M6H/M8H/MAH-XXXSP/FP, there is not this register. Fix to “ 0016.”

Address 00E016

Horizontal Position Register

b7 b6 b5 b4 b3 b2 b1 b0

Horizontal position register (HR) [Address 00E0 16]

B	Name	Functions	After reset	R	W
0 to 5	Horizontal display start positions (HR0 to HR5)	64 steps (0016 to 3F16)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When thses bits are read out, the values are “0.”		0	R	—

Addresses 00E1$_{16}$ and 00E2$_{16}$

Vertical Position Register i

b7 b6 b5 b4 b3 b2 b1 b0

Vertical position register i (CVi) (i = 1 and 2) [Addresses 00E1$_{16}$, 00E2$_{16}$]

B	Name	Functions	After reset	R	W
0 to 6	Vertical display start positions (CVi : CVi0 to CVi6)	128 steps (00$_{16}$ to 7F$_{16}$)	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Address 00E4$_{16}$

Character Size Register

b7 b6 b5 b4 b3 b2 b1 b0

Character size register (CS) [Address 00E4$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Character size of block 1 selection bits (CS10, CS11)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
2,3	Character size of block 2selection bits (CS20,CS21)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address $00E5_{16}$

Border Selection Register

b7 b6 b5 b4 b3 b2 b1 b0

Border selection register (MD) [Address $00E5_{16}$]

B	Name	Functions	After reset	R	W
0	Block 1 OUT1 output border selection bit (MD10)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
1	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
2	Block 2 OUT1 output border selection bit (MD20)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Addresses $00E6_{16}$ to $00E9_{16}$

Color Register i

b7 b6 b5 b4 b3 b2 b1 b0

Color register i (COi) (i = 0 to 3) [Addresses $00E6_{16}$ to $00E9_{16}$]

B	Name	Functions	After reset	R	W
0	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
1	B signal output selection bit (COi1)	0: No character is output 1: Character is output	0	R	W
2	G signal output selection bit (COi2)	0: No character is output 1: Character is output	0	R	W
3	R signal output selection bit (COi3)	0: No character is output 1: Character is output	0	R	W
4	B signal output (background) selection bit (COi4) (See note 1)	0: No background color is output 1: Background color is output	0	R	W
5	OUT1 signal output control bit (COi5) (See notes 1, 2)	0: Character is output 1: Blank is output	0	R	W
6	G signal output (background) selection bit (COi6) (See note 1)	0: No background color is output 1: Background color is output	0	R	W
7	R signal output (background) selection bit (COi7) (See note 2)	0: No background color is output 1: Background color is output	0	R	W

Notes 1: When bit 5 =“0” and bit 4 = “1,” there is output same as a character or border output from pin OUT1.
Do not set bit 5 = “0” and bit 4 = “0.”
2: When only bit 7 =“1” and bit 5 “0,” there is output from pin OUT2.

Address $00EA_{16}$

OSD Control Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register (CC) [Address $00EA_{16}$]

B	Name	Functions	After reset	R	W
0	All-blocks display control bit (CC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Block 1 display control bit (CC1)	0 : Block 1 display off 1 : Block 1 display on	0	R	W
2	Block 2 display control bit (CC2)	0 : Block 2 display off 1 : Block 2 display on	0	R	W
3 to 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
7	$P1_0$/OUT2 pin switch bit (CC7)	0 : $P1_0$ 1 : OUT2	0	R	W

Note: Display is controlled by logical product (AND) between the all-blocks display control bit and each block control bit.

Addresses $00EC_{16}$

OSD Port Control Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD port control register (CRTP) [Address $00EC_{16}$]

B	Name	Functions	After reset	R	W
0	HSYNC input polarity switch bit (HSYC)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	VSYNC input polarity switch bit (VSYC)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R/G/B output polarity switch bit (R/G/B)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	OUT2 output polarity switch bit (OUT2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
4	OUT1 output polarity switch bit (OUT1)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	R signal output switch bit (OP5)	0 : R signal output 1 : MUTE signal output	0	R	W
6	G signal output switch bit(OP6)	0 : G signal output 1 : MUTE signal output	0	R	W
7	B signal output switch bit(OP7)	0 : B signal output 1 : MUTE signal output	0	R	W

Address 00ED$_{16}$

OSD Clock Selection Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

OSD clock selection register (CK) [Address 00ED$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	OSD clock selection bits (CK0,CK1)	b1 b0: Functions 0 0: The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2. 0 1: Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports P3$_3$ and P3$_4$ respectively. — OSD oscillation frequency = f(X$_{IN}$) 1 0: (same as above) — OSD oscillation frequency = f(X$_{IN}$)/1.5 1 1: The clock for OSD is supplied by connecting the following across the pins OSC1 and OSC2. • a ceramic resonator only for OSD • a quartz-crystal oscillator only for OSD and a feedback resistor (See note)	0	R	W
2 to 7	Fix these bits to “0.”		0	R	W

Note: It is necessary to connect other ceramic resonator or quartz-crystal oscillator for OSD across the pins X$_{IN}$ and X$_{OUT}$.

Addresses 00EE$_{16}$

A-D Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0

A-D control register 1 (AD1) [Address 00EE$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADM0 to ADM2)	b2 b1 b0 0 0 0 : A-D1 0 0 1 : A-D2 0 1 0 : A-D3 0 1 1 : A-D4 1 0 0 : A-D5 1 0 1 : A-D6 1 1 0 : Do not set 1 1 1 : Do not set	0	R	W
3	This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	—
5 to 7	Nothing is assigned. This bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address $00EF_{16}$

A-D Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

A-D control register 2 (AD2) [Address $00EF_{16}$]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC0 to ADC5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc ⋮ 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are reed out, the values are “ 0.”		0	R	—

Addresses $00F4_{16}$

Timer 12 Mode Register

b7 b6 b5 b4 b3 b2 b1 b0 (b5 = 0)

Timer mode register (T12M) [Address $00F4_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (T12M0)	0: $f(X_{IN})/16$ 1: $f(X_{IN})/4096$	0	R	W
1	Timer 2 count source selection bit (T12M1)	0: Interrupt clock source 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (T12M2)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (T12M3)	0: Count start 1: Count stop	0	R	W
4	Timer 2 internal count source selection bit 2 (T12M4)	0: $f(X_{IN})/16$ 1: Timer 1 overflow	0	R	W
5	Fix this bit to “0.”		0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address $00F5_{16}$

Timer 34 Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 34 mode register (T34M) [Address $00F5_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (T34M0)	0 : f(X_{IN})/16 1 : External clock source	0	R	W
1	Timer 4 internal interrupt count source selection bit (T34M1)	0 : Timer 3 overflow signal 1 : f(X_{IN})/16	0	R	W
2	Timer 3 count stop bit (T34M2)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (T34M3)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit (T34M4)	0: Internal clock source 1: f(X_{IN})/2	0	R	W
5	Timer 3 external count source selection bit (T34M5)	0: TIM3 pin input 1: HSYNC pin input	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Addresses $00F9_{16}$

Interrupt Input Polarity Register

b7 b6 b5 b4 b3 b2 b1 b0

0 (b7), 0 (b2), 0 (b1)

Interrupt input polarity register(RE) [Address $00F9_{16}$]

B	Name	Functions	After reset	R	W
0	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
1,2	Fix These bits to “0.”		0	R	W
3	INT1 polarity switch bit (RE3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (RE4)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (RE5)	0 : Positive polarity 1 : Negative polarity	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
7	Fix this bit to “0.”		0	R	W

Address 00FB16

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0
1 1 1 1 1 _ 0 0

CPU mode register (CM) [Address 00FB16]

B	Name	Functions	After reset	R	W
0, 1	Fix these bits to “0.”		Indeterminate	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3 to 7	Fix these bits to “1.”		Indeterminate	R	W

Note: This bit is set to “1” after the reset release.

Addresses 00FC16

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	OSD interrupt request bit (CRTR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Multi-master I2C-BUS interface interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	INT3 external interrupt request bit (IT3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻

✻: “0” can be set by software, but “1” cannot be set.

Address 00FD16

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0: 0 (b7 fixed)

Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (IT1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	INT2 external interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5, 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
7	Fix this bit to "0."		0	R	W

✻: "0" can be set by software, but "1" cannot be set.

Addresses 00FE16

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (CRTE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Multi-master I2C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	INT3 external interrupt enable bit (IT3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Address 00FF$_{16}$

Interrupt Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0		0			

Interrupt control register 2 (ICON2) [Address 00FF$_{16}$]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 external interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (S1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Fix this bit to “0.”		0	R	W
4	f(XIN)/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5 to 7	Fix these bits to “0.”		0	R	W

Addresses 021B$_{16}$

ROM Correction Enable Register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0		

ROM correction enable register (RCR) [Address 021B$_{16}$]

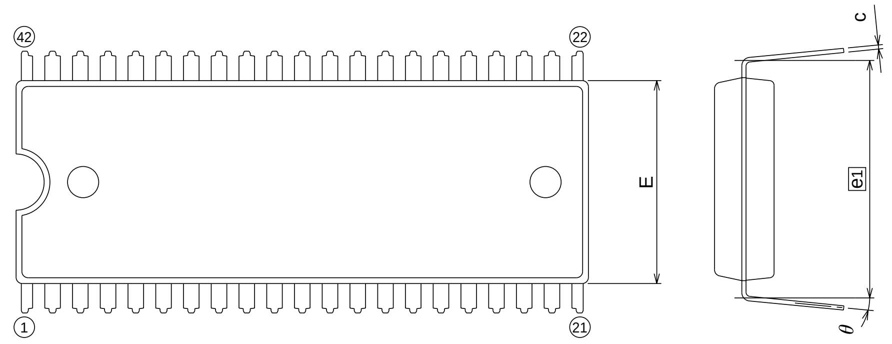
B	Name	Functions	After reset	R	W
0	Vector 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Vector 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to “0.”		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

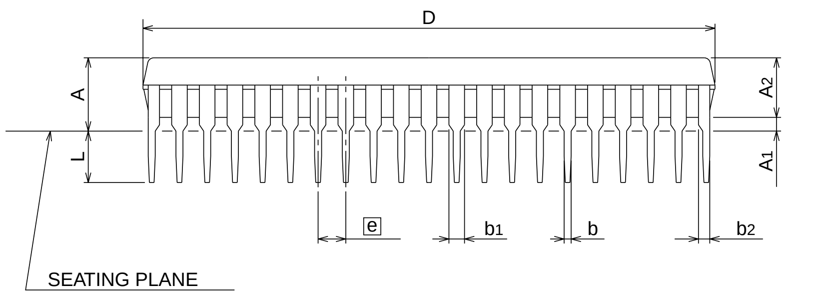
20. PACKAGE OUTLINE

42P4B (MMP)

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy



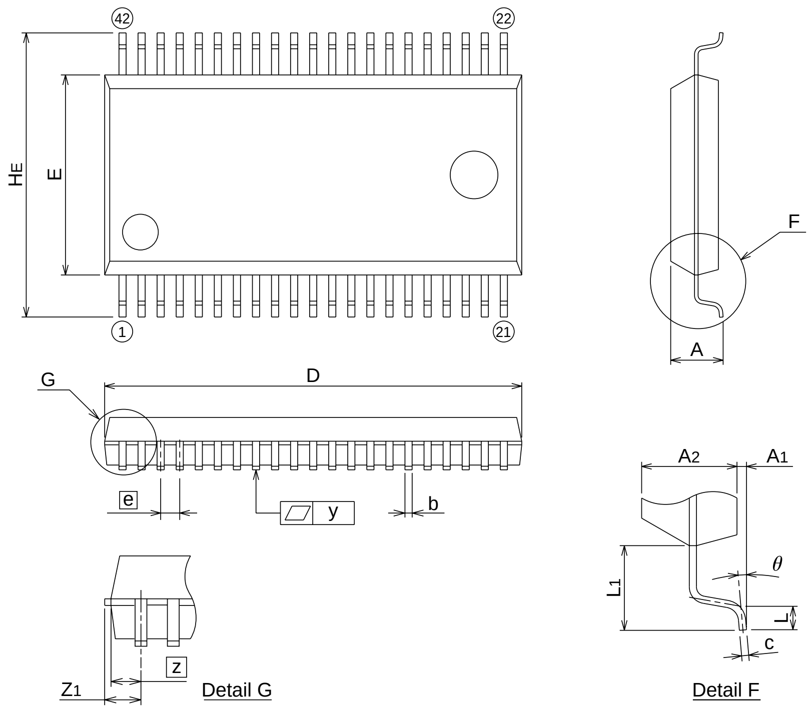


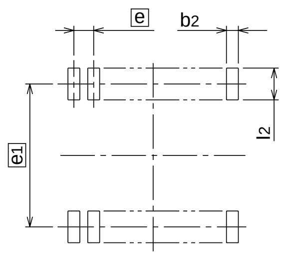
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
e_1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

42P2R-A/E

Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	0.63	Alloy 42





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
z	–	0.75	–
Z_1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
e_1	–	11.43	–
I_2	1.27	–	–

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

RENESAS
Renesas Technology Corp.

REVISION HISTORY	M37221M4H/M6H/M8H/MAH–XXXSP/FP M37221EASP/FP (Rev.1.0) DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	PDF First Edition	0210