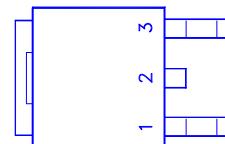
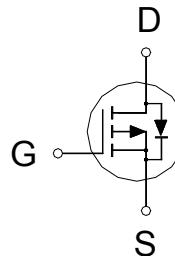


NIKO-SEM P-Channel Logic Level Enhancement Mode Field Effect Transistor P3506DD
TO-252
Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-60V	35mΩ	-26A



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-26	A
		-16	
Pulsed Drain Current ¹	I_{DM}	-100	A
Avalanche Current	I_{AS}	-39	
Avalanche Energy ²	E_{AS}	77	mJ
Power Dissipation	P_D	42	W
		17	
Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	°C / W

¹Pulse width limited by maximum junction temperature.

² $V_{DD} = -30\text{V}$. Starting $T_J = 25^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

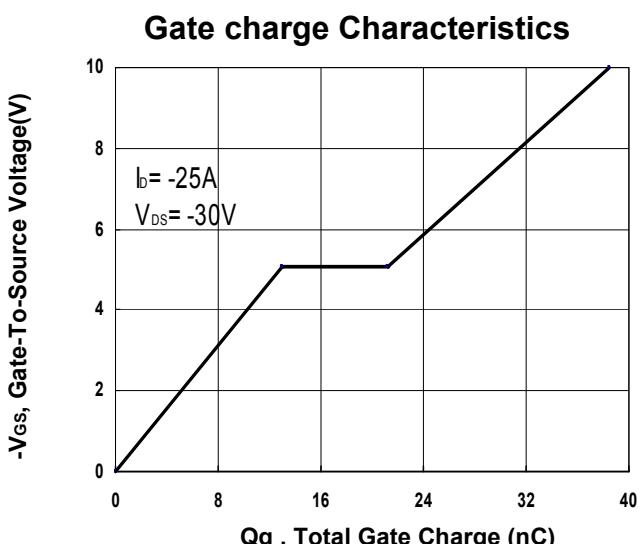
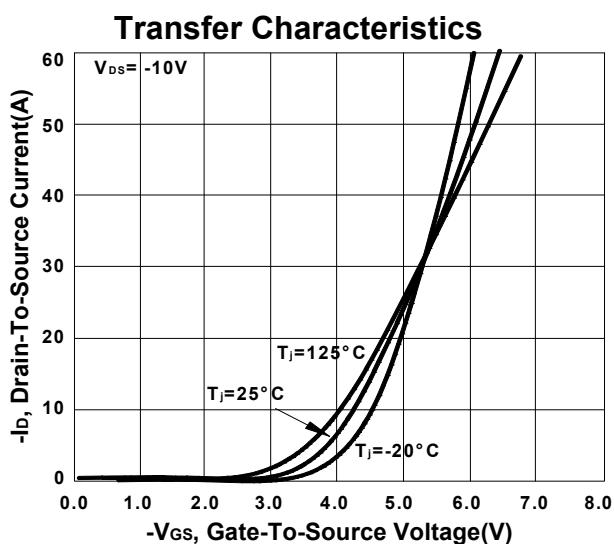
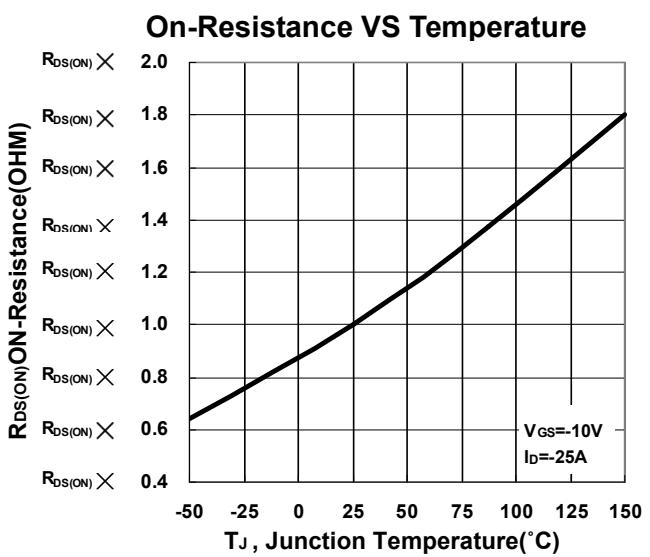
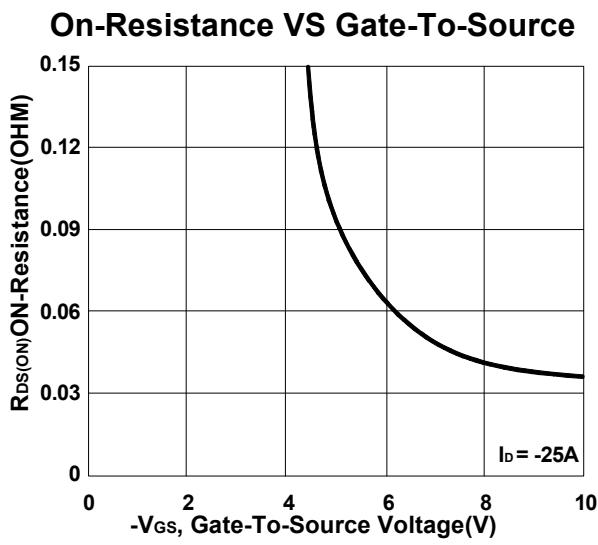
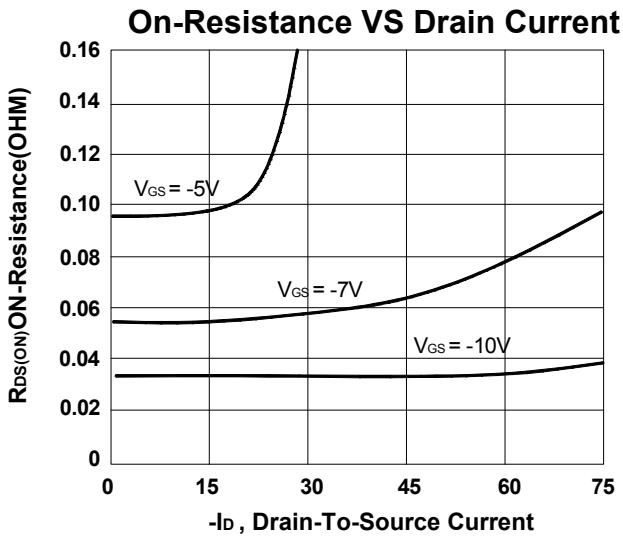
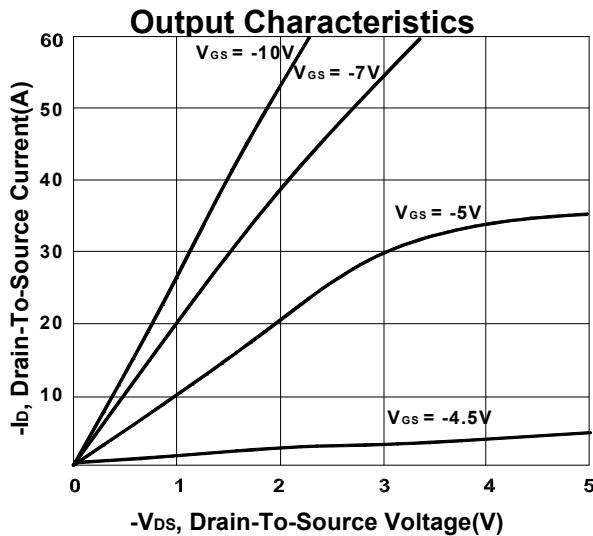
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	-2	-2.7	-4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}$			1	μA
		$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$			10	
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -7\text{V}, I_D = -20\text{A}$		32	55	$\text{m}\Omega$
		$V_{GS} = -10\text{V}, I_D = -25\text{A}$		29	35	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5\text{V}, I_D = -25\text{A}$		15		S

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On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V,$	-100			A
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -30V, f = 1MHz$		2550		pF
Output Capacitance	C_{oss}			241		
Reverse Transfer Capacitance	C_{rss}			140		
Gate Resistance	R_g		$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$	4.85		Ω
Total Gate Charge ²	Q_g	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V, I_D = -25A$		39		nC
Gate-Source Charge ²	Q_{gs}			13		
Gate-Drain Charge ²	Q_{gd}			8		
Turn-On Delay Time ²	$t_{d(on)}$			30		
Rise Time ²	t_r	$V_{DS} = -30V, R_L = 1\Omega$ $I_D \approx -20A, V_{GS} = -10V, R_{GEN} = 6\Omega$		90		nS
Turn-Off Delay Time ²	$t_{d(off)}$			70		
Fall Time ²	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)						
Continuous Current	I_S				-26	A
Forward Voltage ¹	V_{SD}	$I_F = -25A, V_{GS} = 0V$			-1.3	V
Reverse Recovery Time	t_{rr}	$I_F = -25A, dI_F/dt = 100A/\mu S$		30		nS
Reverse Recovery Charge	Q_{rr}			100		nC

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

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