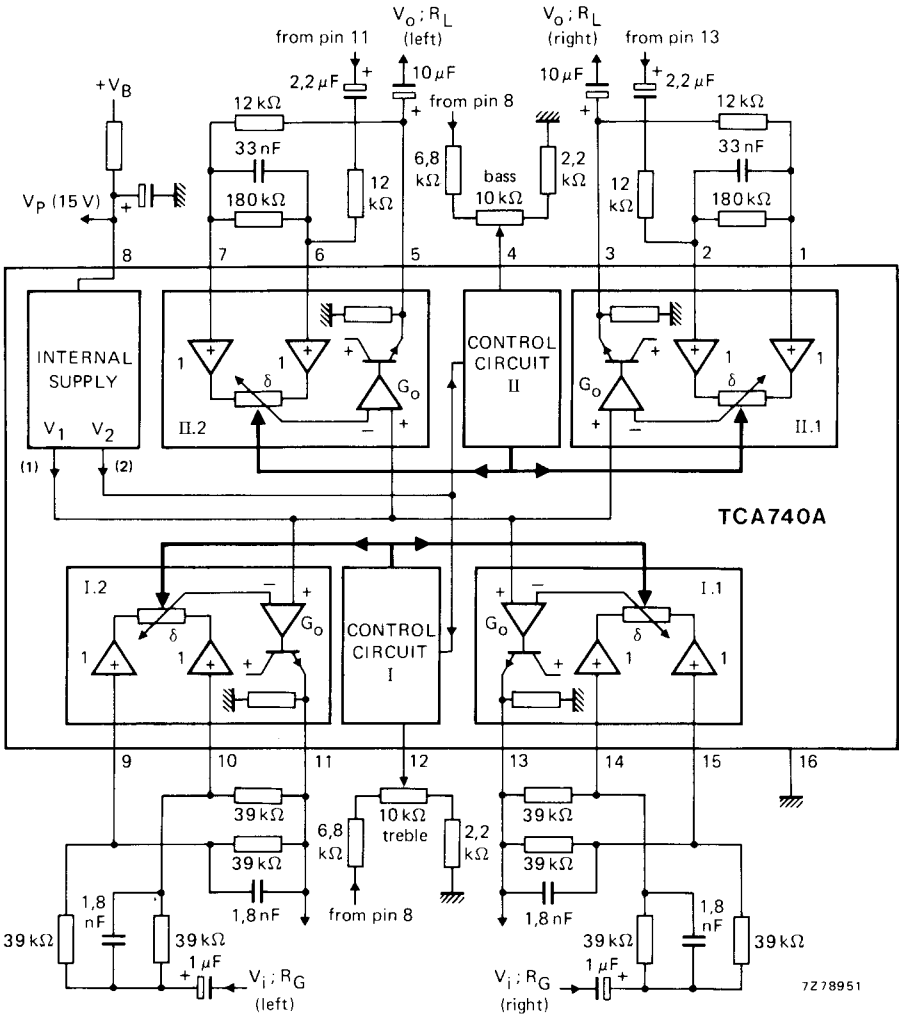


(1) 6,6 V_{BE}; V_1 = 4,6 V

(2) 0,31 V_P + 1,4 V_{BE}; V_2 = 5,6 V

Fig. 1 Block diagram with external circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	V_P	max.	18 V
Control voltages (pins 4 and 12)	$V_{4\text{-}16}$	max.	12 V
	$-V_{4\text{-}16}$	max.	5 V
	$V_{12\text{-}16}$	max.	12 V
	$-V_{12\text{-}16}$	max.	5 V
Total power dissipation	P_{tot}	max.	900 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

CHARACTERISTICS

V_P = 15 V; T_{amb} = 25 °C; measured in Fig.1; in position 'linear' ($V_{4\text{-}16} = V_{12\text{-}16}$ = 5,6 V); R_G = 60 Ω; R_L = 5,6 kΩ; f = 1 kHz; unless otherwise specified

Supply voltage range (pin 8)	V_P		13,5 to 16,5 V
Supply current (pin 8)	I_P	typ.	34 mA
			25 to 45 mA
Signal processing			
Voltage gain at linear frequency response	G_v	typ.	0 dB
Frequency response (−1 dB)	f		20 Hz to 20 kHz
Maximum gain variation at f = 1 kHz at maximum bass/treble boost or cut	ΔG_v	<	± 1,5 dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 9,2 V		>	15 dB
		typ.	16 dB
Bass cut at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 2 V		>	15 dB
		typ.	16 dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 9,2 V		>	15 dB
		typ.	16 dB
Treble cut at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 2 V		>	15 dB
		typ.	16 dB
Total distortion			
$V_{o(rms)}$ = 100 mV; f = 1 kHz	d_{tot}	typ.	0,03 %
$V_{o(rms)}$ = 100 mV; f = 40 Hz to 16 kHz	d_{tot}	typ.	0,1 %
$V_{o(rms)}$ = 1 V; f = 1 kHz	d_{tot}	typ.	0,07 %
		<	0,2 %
$V_{o(rms)}$ = 1 V; f = 40 Hz to 16 kHz	d_{tot}	typ.	0,2 %
Input/output voltage at d_{tot} = 0,7 % (r.m.s. value)	$V_{i(rms)} = V_{o(rms)}$	>	1,6 V
		typ.	2 V
Output signal plus noise voltage (r.m.s. value) f = 20 Hz to 20 kHz	$V_{no(rms)}$	typ.	40 μV
Output noise voltage; weighted conform DIN45405; peak value	$V_{no(m)}$	typ.	90 μV
		<	160 μV

CHARACTERISTICS (continued)

Channel separation				
f = 1 kHz		α	typ.	72 dB
f = 250 Hz to 12,5 kHz		α	typ.	68 dB
f = 40 Hz to 16 kHz		α	>	50 dB
			typ.	58 dB
Control voltages				
Recommended control voltage range			>	0 V
treble/bass	$V_{4-16} = V_{12-16}$			2 to 9,2 V
			<	0,66 V_P V
			typ.	5,6 V
Control voltage at linear frequency response	$V_{4-16} = V_{12-16}$			5,4 to 5,8 V
				(0,31 V_P to 1,4 V_{BE}) V
Quiescent input current			typ.	6 μA
$V_{4-16} = V_{12-16}$ = 2 to 9,2 V	$I_4 = I_{12}$		<	25 μA
Input resistance (pins 4 and 12)				
$V_{4-16} = V_{12-16}$ = 5,6 V	$R_{i4;12}$		typ.	800 kΩ
Amplifier characteristics				
Quiescent input currents; V_i = 4,6 V			typ.	0,6 μA
(pins 1, 2, 6, 7, 9, 10, 14 and 15)	$I_1;I_2;I_6;I_7;I_9;I_{10};I_{14};I_{15}$		<	2 μA
Input resistance (pins 1,2,6,7,9,10,14 and 15)	$R_{i\ 1;2;6;7;9;10;14;15}$		>	1 MΩ
Internal emitter resistance at outputs	R_{3-16}; R_{5-16}; R_{11-16}; R_{13-16}		typ.	2 kΩ
Output resistance (pins 3,5,11 and 13)	$R_{o\ 3;5;11;13-16}$		typ.	10 Ω
Maximum gain; no load		G_v	>	40 dB
			typ.	43 dB
D.C. output voltages			typ.	4,6 V
$V_{4-16} = V_{12-16}$ = 5,6 V (pins 3,5,11 and 13)	V_{3-16}; V_{5-16}; V_{11-16}; V_{13-16}			4,3 to 4,9 V
				(6,6 V_{BE}) V

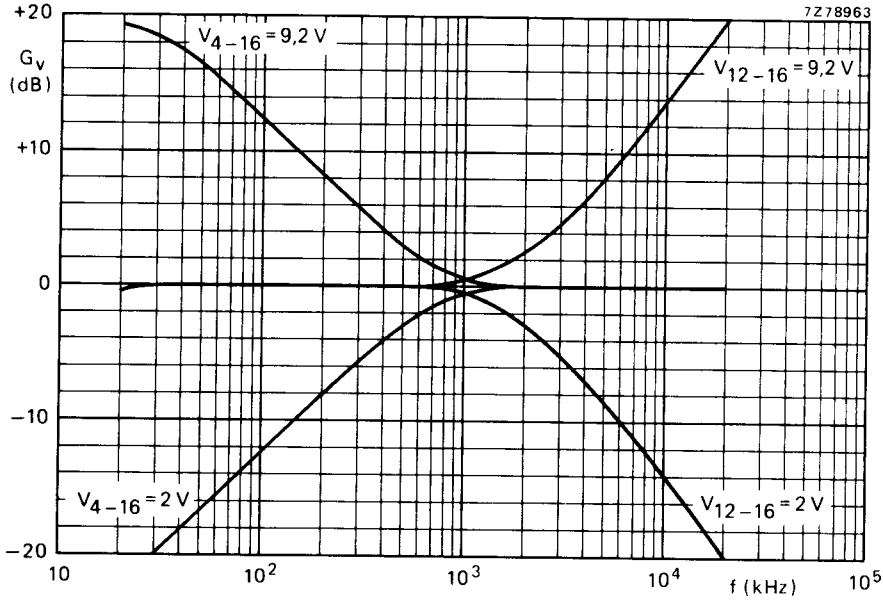


Fig. 2 Frequency response.

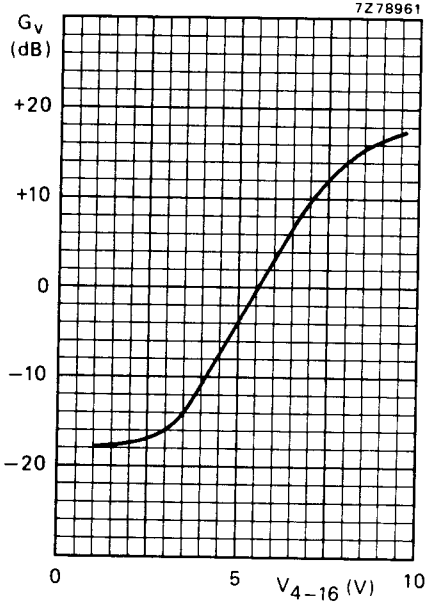


Fig. 3 Bass control curve at f = 40 Hz.

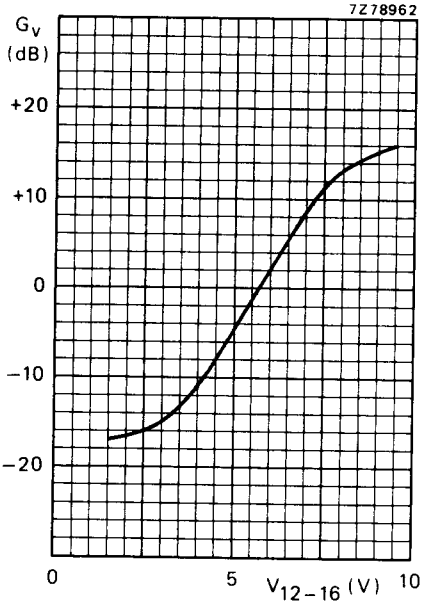


Fig. 4 Treble control curve at f = 16 kHz.

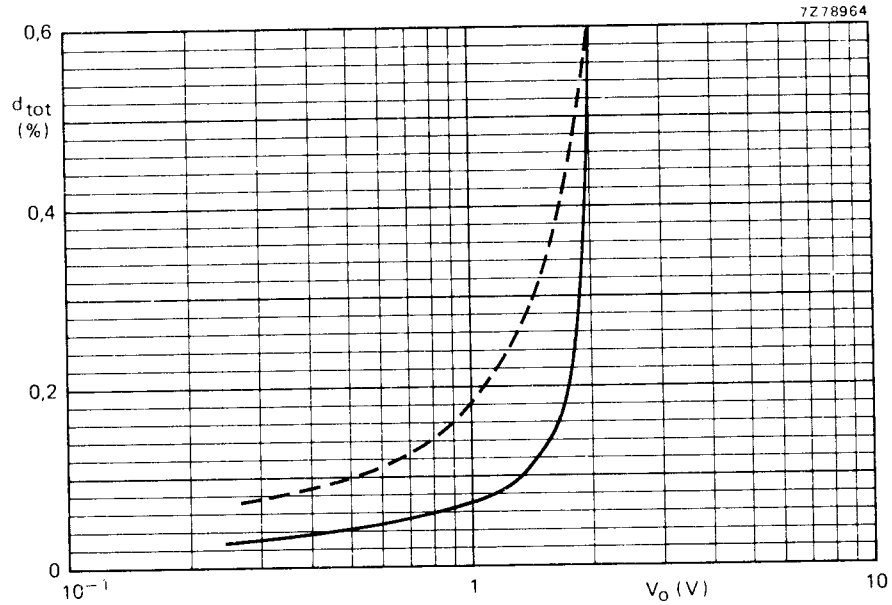
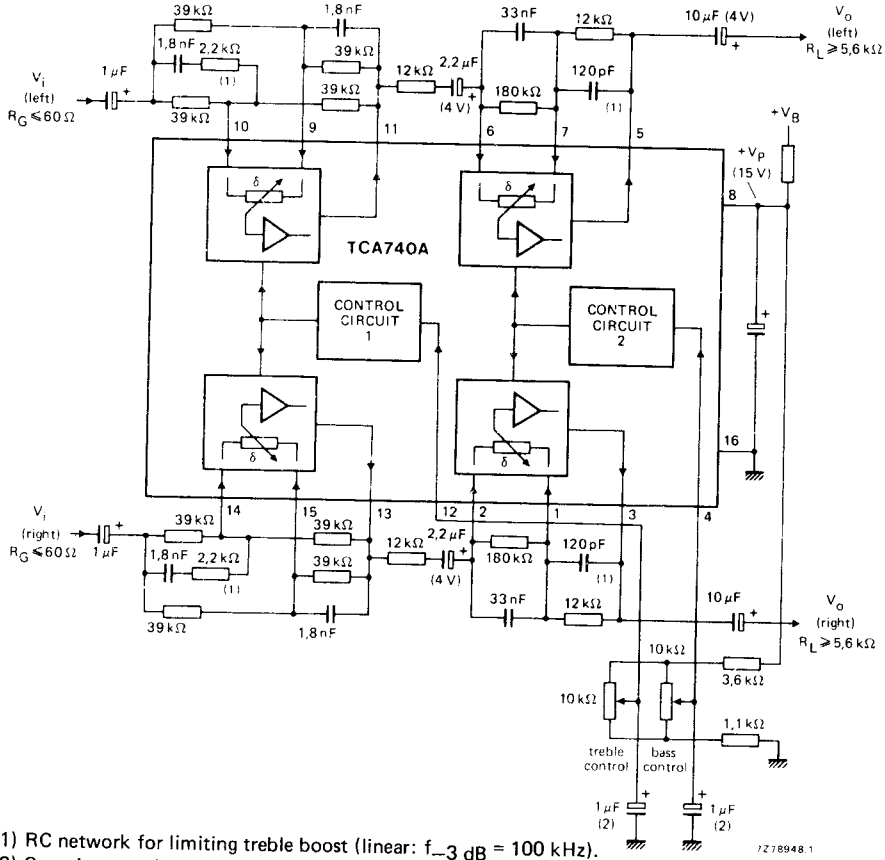


Fig. 5 Total distortion as a function of output voltage; $V_{4\text{-}16} = V_{12\text{-}16} = 5{,}6$ V (linear, $G_{V\,tot} = 1$); ——— f = 1 kHz; – – – f = 40 Hz to 16 kHz.

APPLICATION INFORMATION



(1) RC network for limiting treble boost (linear: $f_{-3\ dB} = 100$ kHz).
(2) Capacitors are intended for suppression of the noise when adjusting the mechanical potentiometers.

Fig. 6 Application example of TCA740A used for treble and bass control.

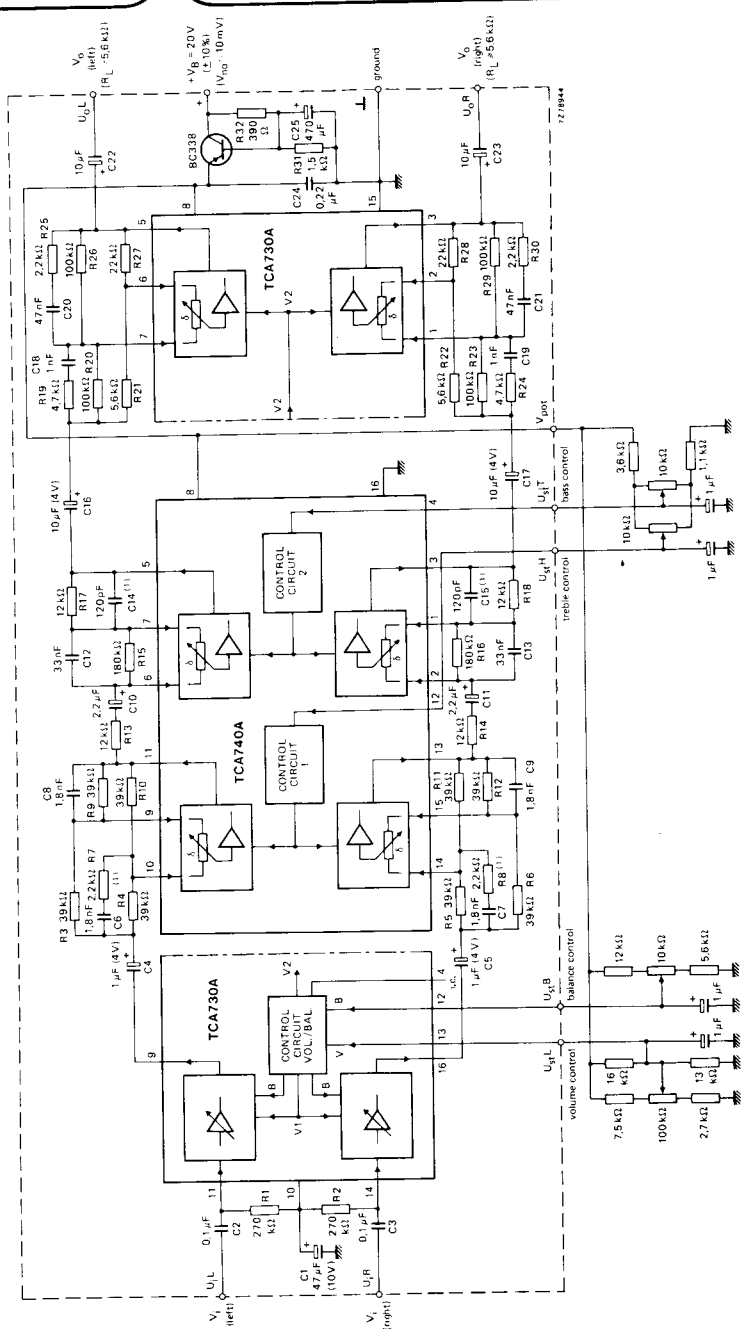


Fig. 7 Application diagram for TCA730A and TCA740A.
For printed-circuit board see Fig. 8.

(1) RC network for limiting treble boost (linear: f_−3 dB = 100 kHz).

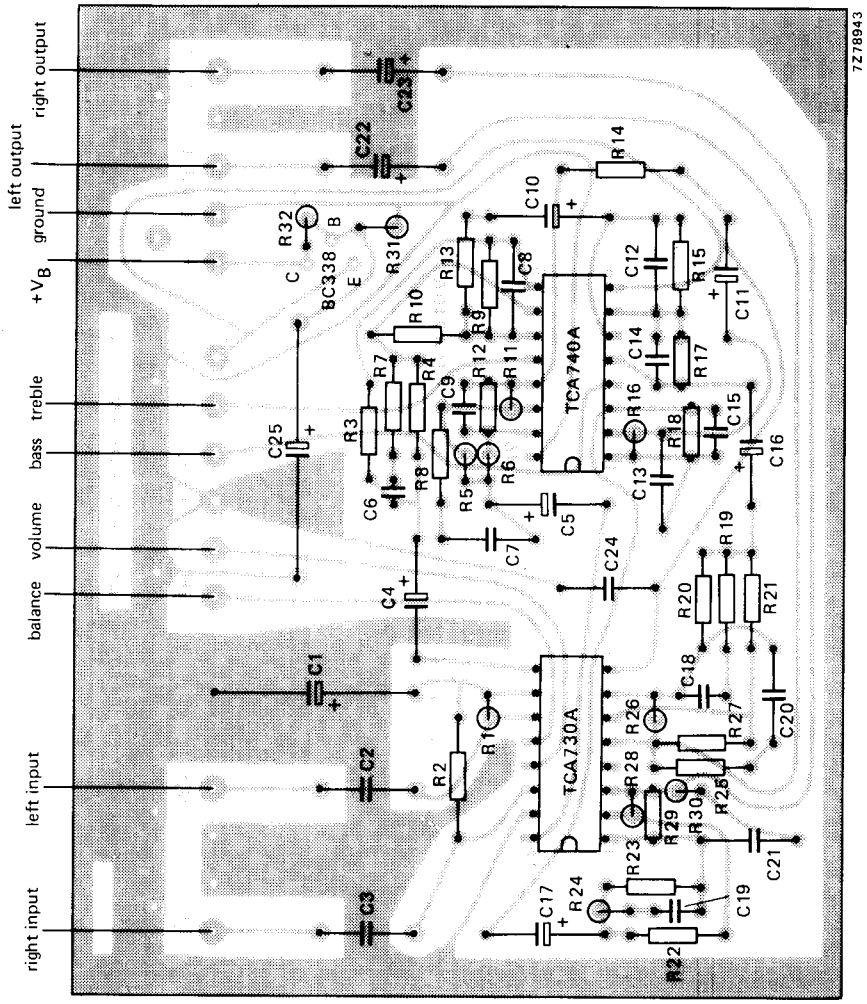


Fig. 8 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 7.