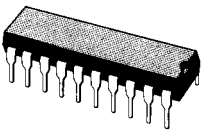
HIGH EFFICIENCY AUDIO PWM DRIVER

- HIGH EFFICIENCY
- P_o = 30 W WITH POWER MOS BRIDGE
- LOW DISTORTION
- SINGLE SUPPLY OPERATION
- MUTING FACILITY
- THERMAL AND SHORT-CIRCUIT PROTECTION
- DUMP PROTECTION



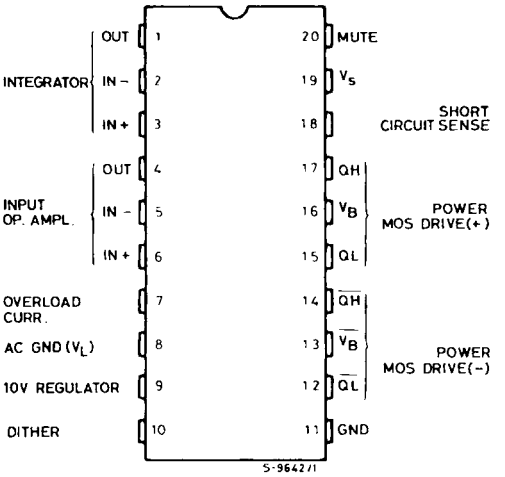
DIP - 20
(Plastic 0.4)

ORDER CODE : TDA7260

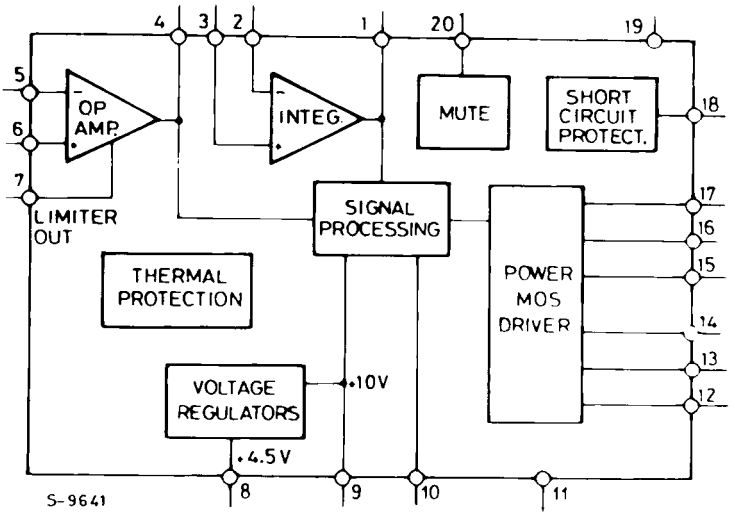
DESCRIPTION

The TDA7260 is a new type of audio driver mainly intended for use in car radio applications. In conjunction with four POWER MOS in bridge configuration it can deliver 30W (d 3% R_L = 2 Ω). The device acts in "class D" as a pulse width modulation circuit. That permits a very high efficiency (> 80% at rated output power) so no heatsinks are needed. Moreover, a built-in limiter reduces the clipping effects. The TDA7260 is a monolithic integrated circuit in a 20 lead dual in line plastic package.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	30	V
V_s	Peak Supply Voltage (50 ms)	40	V
V_{IN}	Input Voltage	10	V
V_D	Differential Input Voltage	± 6	V
I_P	Peak Output Current	300	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W

TEST CIRCUITS

Figure 1.

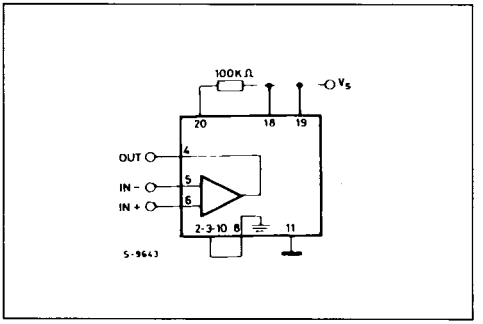


Figure 2.

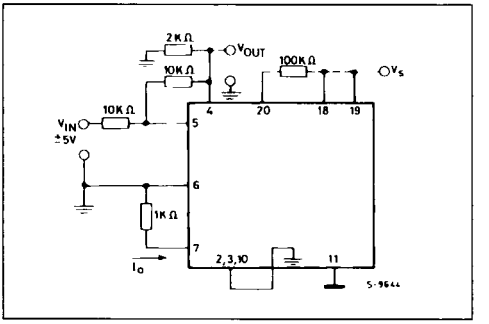


Figure 3.

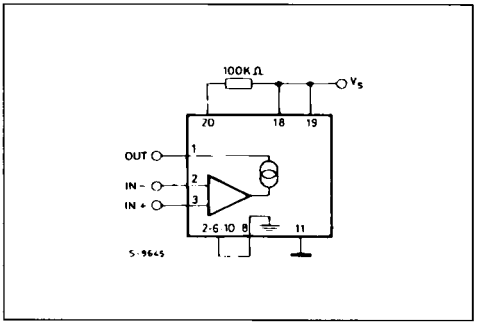


Figure 4.

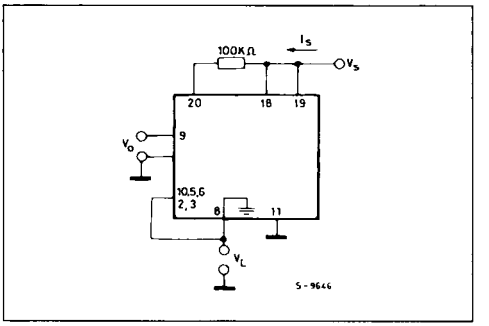


Figure 5.

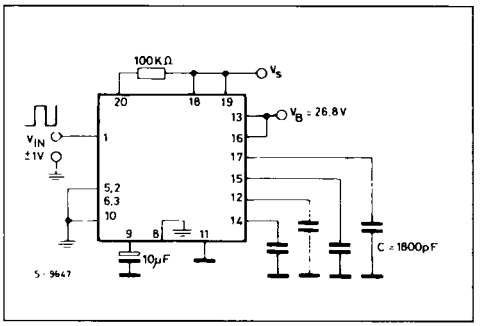
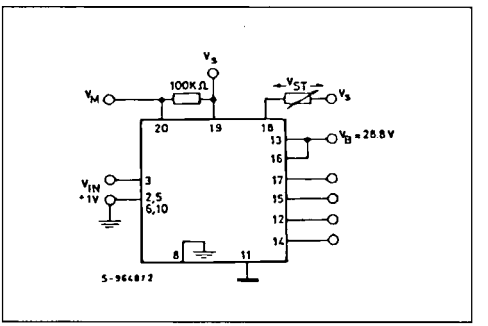


Figure 6.



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_s = 14.4 V unless otherwise specified, refer to test circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
OP AMP							
V_{os}	Input Offset Voltage				± 4	mV	1
I_b	Input Bias Current			120	300	nA	1
I_{of}	Input Offset Current				± 50	nA	1
G_v	Open Loop Voltage Gain		80			dB	1
d	Total Harmonic Distortion	f = 1 kHz A_v = 1		0.005		%	1
BW	Unity Gain Bandwith		0.8	1.8		MHz	1
CMRR	Common Mode Rejection	V_{IN} = 1 V f = 1 kHz	70	90		dB	1
SVR	Supply Voltage Rejection	V_r = 1 V f = 1 kHz	80	100		dB	1
E_n	Input Noise Voltage	B = 20 kHz		1		mV	1
I_n	Input Noise Current	B = 20 kHz		20		nA	1
SR	Slew Rate			0.8		V /ms	1
V_O	Output Swing	R_L = 2 KΩ A_v = 1	± 2.6		± 3.2	V	2
R_{IN}				100		kΩ	1
I_7	Overload Indicator Current			240		mA	2
INTEGRATOR							
V_{os}	Input Offset Voltage				± 4	mV	3
I_b	Input Bias Current			0.5	2.5	µA	3
I_{of}	Input Offset Current				± 250	nA	3
I_o	Output Current Swing Sink Source	 ΔV_{IN} = ± 1 V R_L = 0	 0.4 0.4	 1 1		 mA mA	3
V_o	Output Voltage Swing	ΔV_{IN} = ± 1 V R_L = 5 kΩ	± 3			V	3
CMRR	Common Mode Rejection	V_{IN} = 1 V f = 1 kHz	70	90		dB	3
SVR	Supply Voltage Rejection	V_r = 1 V f = 1 kHz	80	100		dB	3
R_{IN}			100			kΩ	3
BW	Unity Gain Bandwith			4		MHz	3
G_n	Forward Transconductance			30		mA/V	3
REGULATORS							
V_o	Output Stabilized Voltage			10		V	4
SVR	Supply Voltage Rejection	f = 1kHz V_r = 1 V	60	70		dB	4
V_I	Ground Voltage			4.5		V	4

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYSTEM SPECIFICATION							
V_s	Operating Supply Voltage Range	See Fig. 24		(10.5 to 16)		V	
I_s	Supply Current	V_{IN} = 0		30	60	mA	4
V_{tm}	Mute Threshold Voltage (*)	V_{IN} = 0	3	4	5.5	V	6
V_{tmh}	Mute Threshold Hysteresis	V_{IN} = 0		0.5		V	6
$V_{o\,H}$	Output Swing (QH, $\overline{QH}$),	I = 70 mA	25			V	6
$V_{o\,H}$	Output Swing (QL, $\overline{QL}$)	I = 70 mA	10.8			V	6
$V_{o\,L}$	Output Swing (QH, $\overline{QH}$)	I = 70 mA			2.8	V	6
$V_{o\,L}$	Output Swing (QL, $\overline{QL}$)	I = 70 mA			2.8	V	6
V_{st}	Overload Sense Threshold		0.2		0.4	V	6
V_{om}	Muted Outputs	I = 70 mA Mute or Overload Condition			2.8	V	6
V_x	Gate Crossover Voltage	f = 1 kHz		2		V	5
COMPLETE SYSTEM							
I_o	Supply Current	V_{IN} = 0 R_L = ∞		90		mA	7
V_{of}	Output Offset Voltage	V_{IN} = 0		5		mV	7
CMRR	Common Mode Ripple Rejection	V_{IN} = 0.5 V f = 100 Hz		60		dB	7
SVR	Supply Voltage Ripple Rejection	ΔV_R = 0.5 V f = 100 Hz		60		dB	7
G_V	Voltage Gain	P_o = 1 W f = 1 kHz		12		dB	7
E_n	Output Noise Voltage	B = 20 kHz V_{IN} = 0		150		μV	7
P_o	Output Power	d = 2 % f = 1 kHz		32		W	7
d	Total Harmonic Distortion	f = 1 kHz Vo = 2 V		0.4		%	7
f_s	Switching Frequency	V_{IN} = 2 V $V_{10} = V_8$	70	125		kHz	7
f_d	Dither Frequency			20		Hz	7
η	Efficiency	P_o = 32 W f = 1 kHz		85		%	7

(*) Device on for V_{pin} 20 higher than V_{tm}.

Figure 7 : Application Circuit.

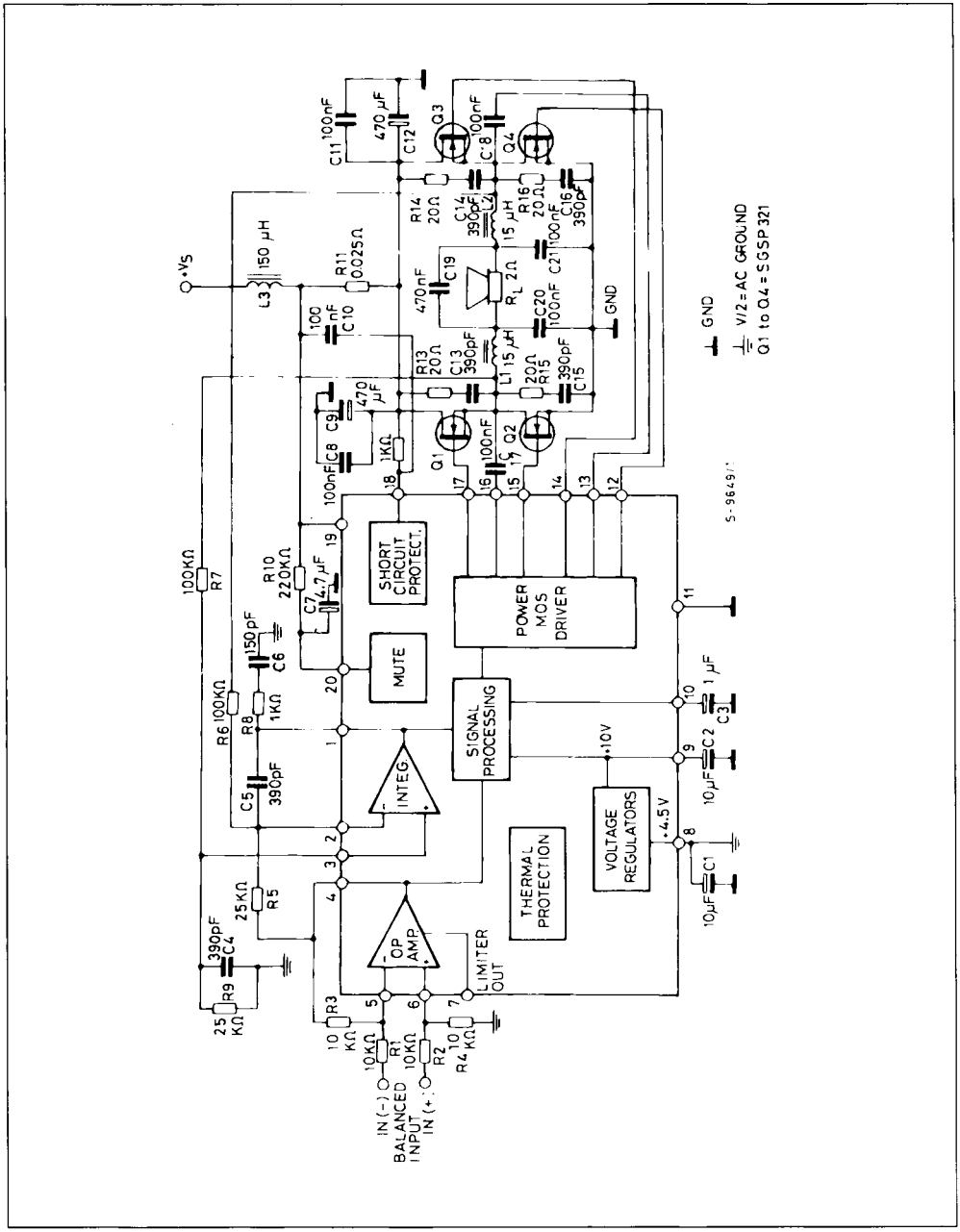


Figure 7a : P.C. Board and Components Layout of the Circuits of Fig. 7 (1 : 1 scale).

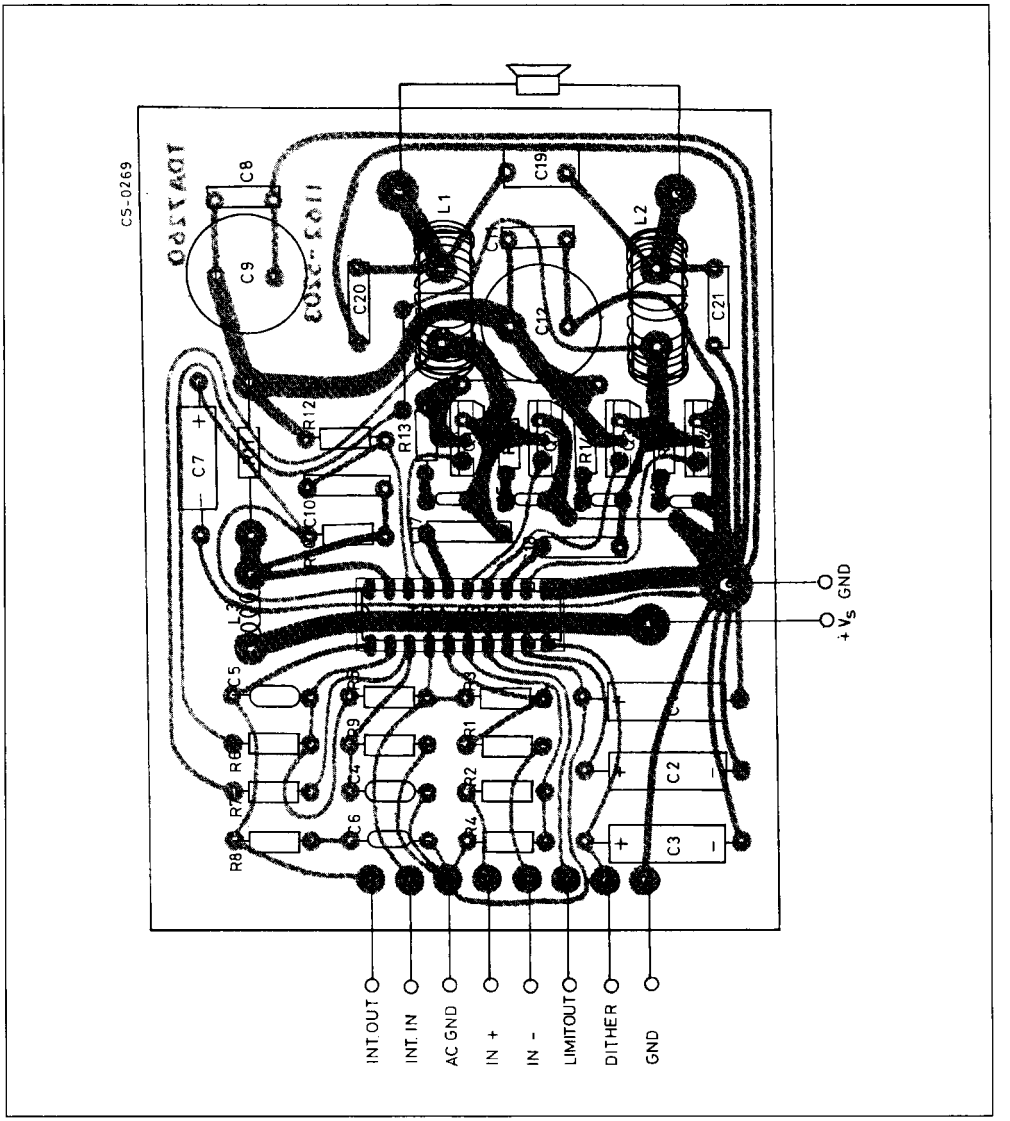


Figure 8 : Quiescient Current vs. Supply Voltage.

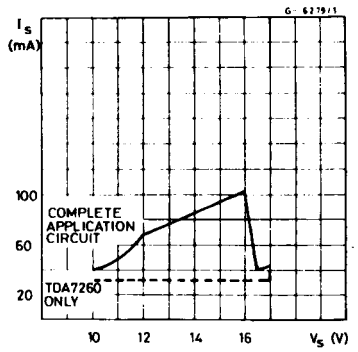


Figure 9 : Distortion vs. Output Power.

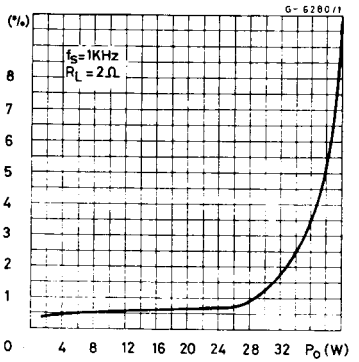


Figure 10 : Distortion vs.Frequency.

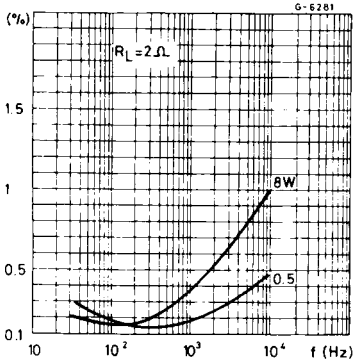


Figure 11 : Frequency Response.

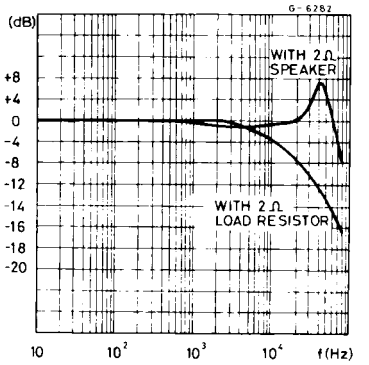


Figure 12 : Dither Frequency Versus $C_{(PIN\ 10)}$.

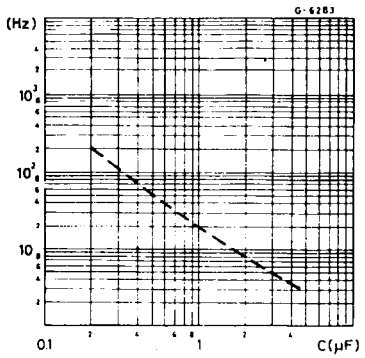


Figure 13 : Efficiency vs. Output Power.

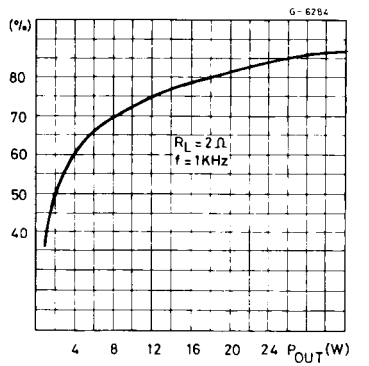


Figure 14 : Power Dissipation vs. Output Power.

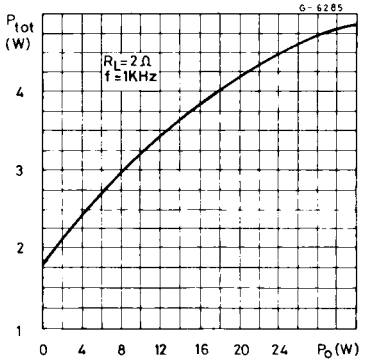


Figure 15 : Suggested Application Circuit Using the TDA7232 Preamplifier/Compressor.

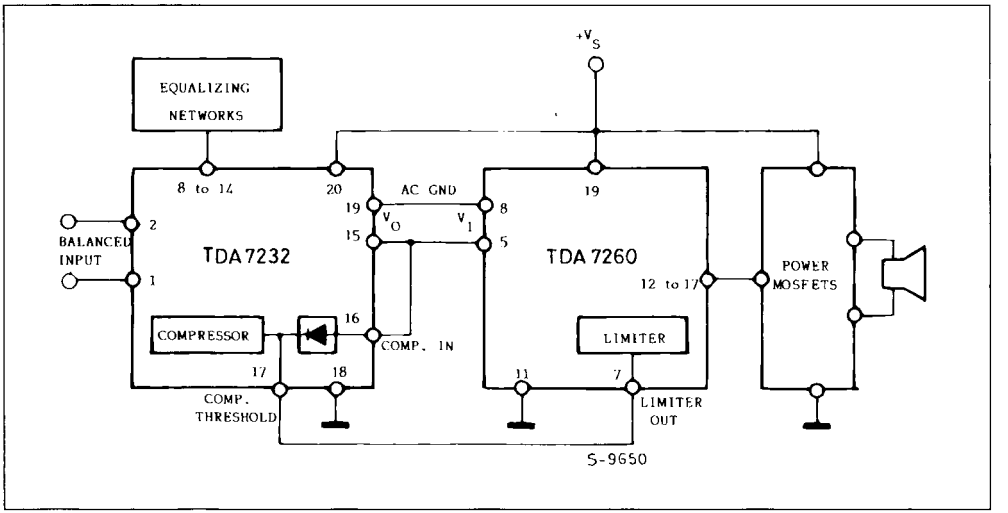


Figure 16 : 25 W Application Circuit.

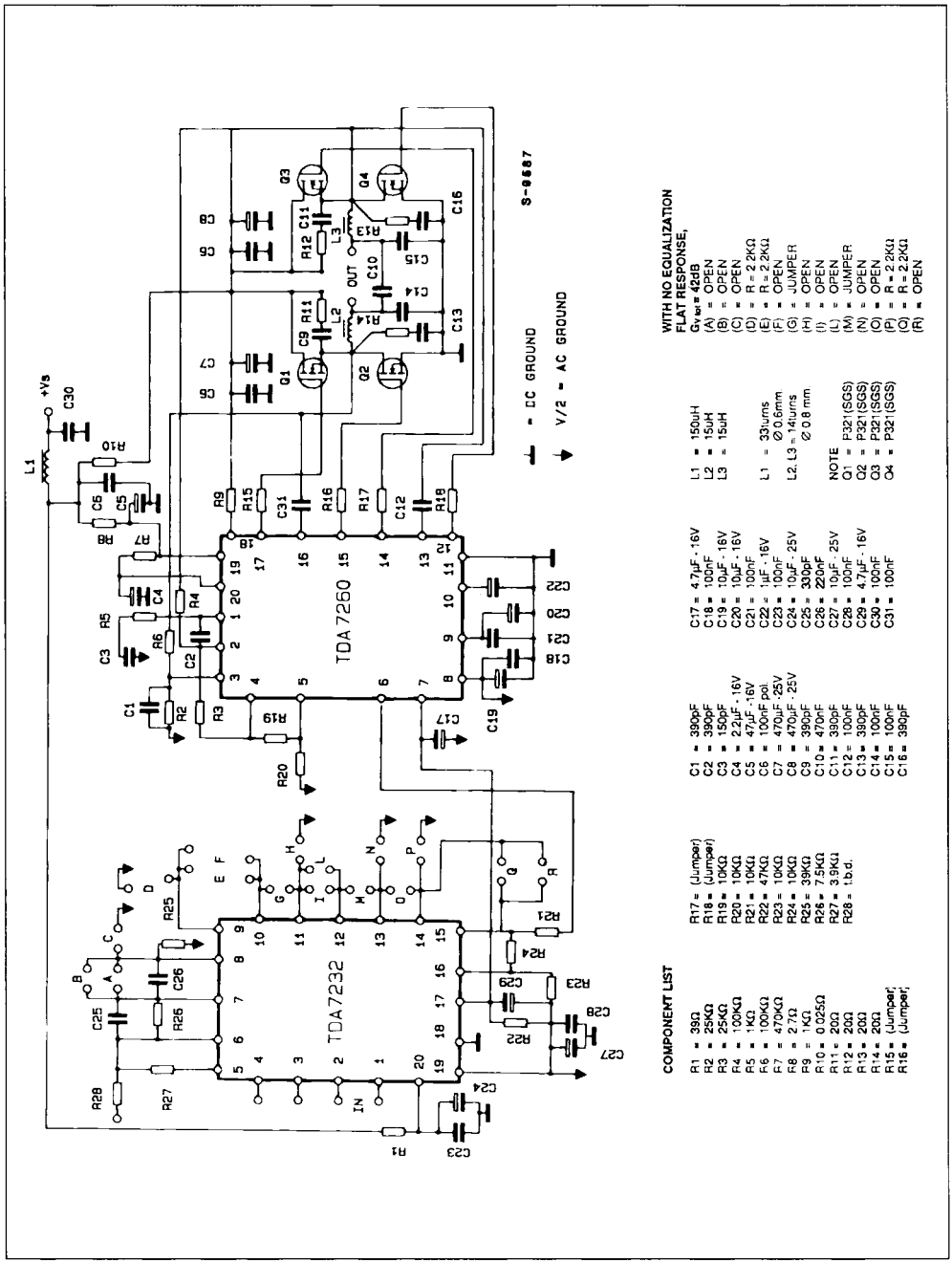
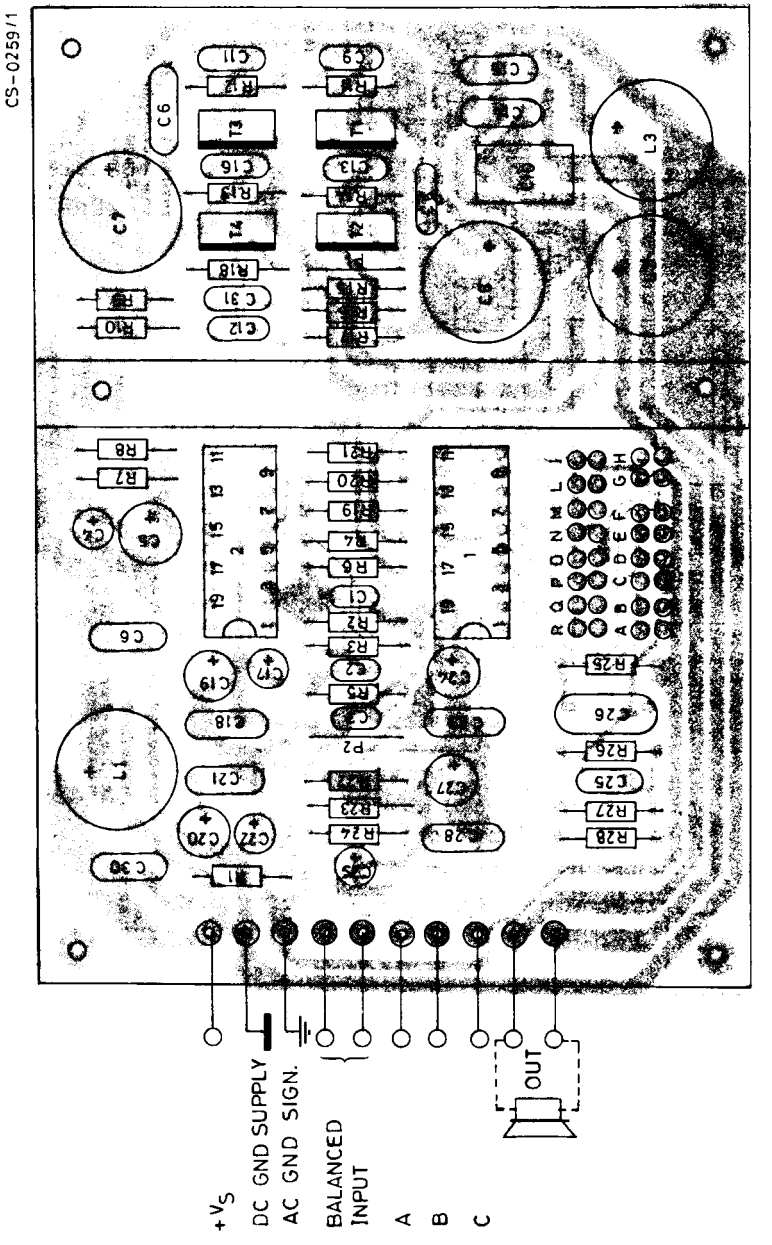
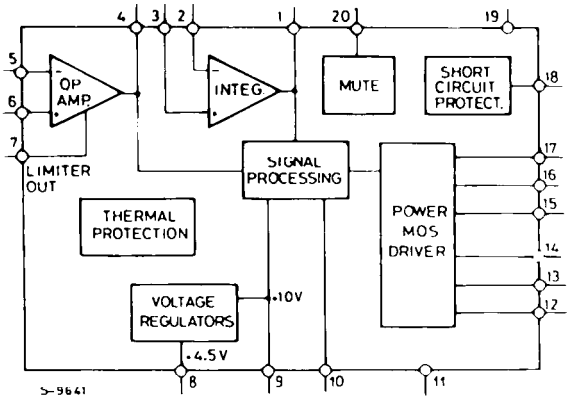


Figure 17 : P.C. Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



APPLICATION INFORMATION

Figure 18 : Block Diagram.



CIRCUIT DESCRIPTION

BLOCK DIAGRAM. Fig. 18 shows the circuit block diagram. Following are described the single circuit blocks and their functions.

VOLTAGE REGULATOR. It generates two values of reference voltage, accessible even on external pins. 10 V is the voltage that supplies all the analogic internal blocks. 4,5 V (V1) is the voltage value which stands for ground of the signal inside the chip.

INPUT AMPLIFIER, INTEGRATOR, COMPARATOR WITH HYSTERESIS, N-FET BLOCK DRIVER. These components implement the control system main loop, together with the external four power devices. The TSM (two state modulation) system is used.

The input amplifier is utilized in differential configuration, and refers the input signal to V1 voltage; in such way the chip turns to general use. On the input amplifier acts a dynamic limiter circuit, with intervention proportional to supply voltage avoiding overload and aliasing at lower V_S (Fig. 19).

Figure 19 : Duty Cycle Input Dynamic Limitation.

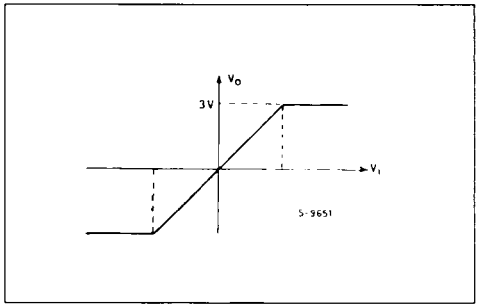
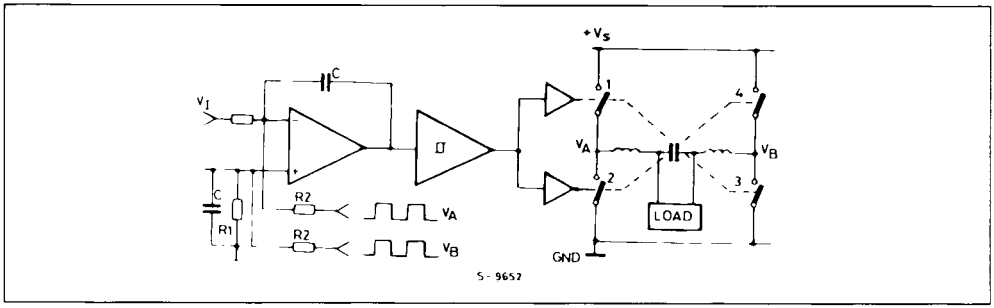


Figure 20 : Free Running Oscillator Principle.

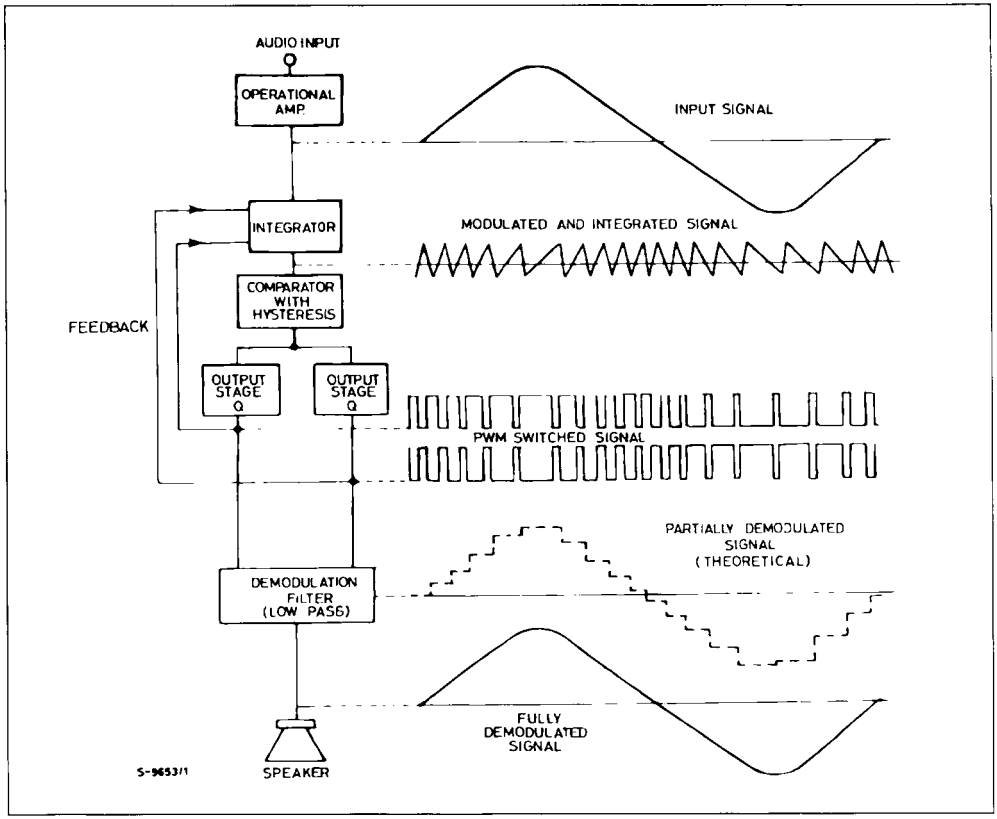


A signal for supplying an external compressor stage (i.e. TDA7232) is available.

For the effective control loop the feedback signal is taken from switched points of external power bridge (before LC output demodulation filter) and sent to the integrator (see Fig. 20).

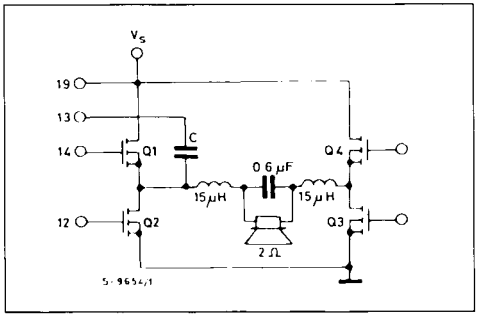
The triangle waveform at the integrator outpout drives the comparator with a hysteresis, and this supplies the correct time-intervals to the driving stages (Fig. 21).

Figure 21.



When an audio signal is introduced to the integrator, it generates an offset which varies the duty cycle and frequency of the switching output (with no audio signal the duty cycle is 50%). The bridge POWER MOS with the drain connected to the supply voltage, are driven in boostrap. The choice of MOS device is suggested by the high commutation speed and in order to reduce the chip dissipation. The Mosfets SGSP321 can be succesfully used. The LC filter on the bridge output demodulates the signal and reconstructs the sine wave on the speaker (see Fig. 22).

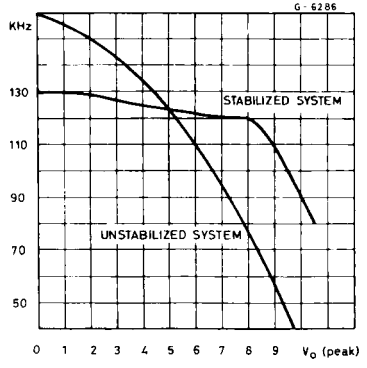
Figure 22.



SWITCHING FREQUENCY STABILIZER. It consists of a block which stabilizes the witching frequency of the system; it receives the supply voltage and the input signal amplitude as inputs, and accomplishes its function by varying the histeresis thresholds of the comparator. The purpose of such stabilizer is to reduce the range of the switching frequency (40KHz < F_{sw} < 200 KHz) avoiding greather variations versus supply voltage, input signal, output current. (Fig. 23).

DITHER OSCILLATOR. It is a low-frequency oscillator. Its frequency (20Hz typ.) is set by an external capacitor; at this value it determines a frequency switching modulation of about 10% around its nominal value, in order to minimize the problem of the spurious irradiations of the harmonics at the switching frequency (EMI).

Figure 23.



MUTE.It is a protection circuit which shuts the system off when the supply voltage is lower than 10.5 V and higher than 16 V. The switching-on is further delayed by an external capacitor. In mute condition the outputs are low (Figs. 24,25).

SHORT CIRCUIT PROTECTION. It is a comparator having an offset which senses the current drawn by the power stage by a voltage drop across an external resistor (internal V_{TH} = 250 mV): it acts on the mute circuit.

THERMAL AND DUMP PROTECTIONS. It shuts the device off when the junction temperature rises above 150 °C, and it has a hysteresis of above 20 °C typ. It acts on the mute circuit.

The device is protected against supply overvoltages (V_S = 40 V, t = 50 ms).

Figure 24.

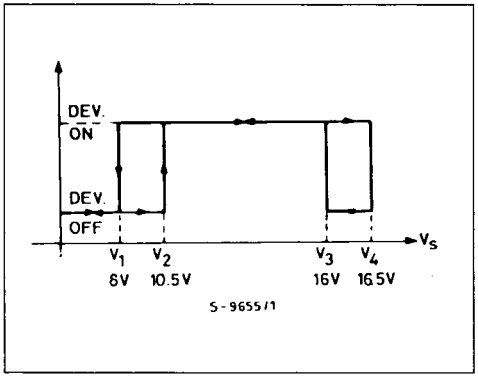


Figure 25.