



# LC863532A/28A/24A/20A/16A

## 8-Bit Single-Chip Microcontroller

### Preliminary

#### Overview

The LC863532/28/24/20/16A are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424μs
- On-chip ROM capacity
  - Program ROM : 32K/28K/24K/20K/16K bytes
  - CGROM : 16K bytes
- On-chip RAM capacity : 512 bytes
- OSD RAM : 352 × 9 bits
- Closed-Caption TV controller and the on-screen display controller
- Four channels × 6-bit AD Converter
- Three channels × 7-bit PWM
- Two channels × 16-bit timer/counter, 14-bit base timer
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 12-source 8-vectored interrupt system
- Integrated system clock generator and display clock generator
  - Only one X'tal oscillator (32.768kHz) for PLL reference is used for both generators
  - TV control and the Closed Caption function

All of the above functions are fabricated on a single chip.

Note : This product includes the IIC bus interface circuit. If you intend to use the IIC bus interface, please notify us of this in advance of our receiving your program ROM code order.  
 Purchase of SANYO IIC components conveys a license under the Philips IIC Patents Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

Trademarks  
 IIC is a trademark of Philips Corporation.

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

## Features

- (1) Read-Only Memory (ROM) : 32768 × 8 bits / 28672 × 8 bits / 24576 × 8 bits  
 20486 × 8 bits / 16384 × 8 bits for program  
 16128 × 8 bits for CGROM
- (2) Random Access Memory (RAM) : 384 × 8 bits (working area)  
 128 × 8 bits (working or ROM correction function)  
 352 × 9 bits (for CRT display)
- (3) OSD functions
- Screen display : 36 characters × 16 lines (by software)
  - RAM : 352 words (9 bits per word)
    - Display area : 36 words × 8 lines
    - Control area : 8 words × 8 lines
  - Characters
    - Up to 252 kinds of 16 × 32 dot character fonts  
 (4 characters including 1 test character are not programmable)
    - Each font can be divided into two parts and used as two fonts (Ex. 16 × 16 dot character font × 2)
    - At least 111 characters need to be divide between a 16×18 dot and 8 × 9 dot character font to display the caption fonts.
  - Various character attributes
    - Character colors : 16 colors (analog mode:  $I_{V_{p-p}}$  output) / 8 colors (digital/mode)
    - Character background colors : 16 colors (analog mode:  $I_{V_{p-p}}$  output) / 8 colors (digital/mode)
    - Fringe / shadow colors : 16 colors (analog mode:  $I_{V_{p-p}}$  output) / 8 colors (digital/mode)
    - Full screen colors : 16 colors (analog mode:  $I_{V_{p-p}}$  output) / 8 colors (digital/mode)
    - Rounding
    - Underline
    - Italic character (slanting)
  - Attribute can be changed without spacing
  - Vertical display start line number can be set for each row independently (Rows can be overlapped)
  - Horizontal display start position can be set for each row independently
  - Horizontal pitch (bit 9 - 16)<sup>\*1</sup> and vertical pitch (bit-32) can be set for each row independently
  - Different display modes can be set for each row independently
    - Caption • Text mode / OSD mode 1 / OSD mode 2 (Quarter size) / Simplified graphic mode
  - Ten character sizes <sup>\*1</sup>
    - Horez. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4), (0.5 × 0.5)  
 (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4), (0.75 × 0.5)
  - Shuttering and scrolling on each row
  - Simplified Graphic Display
- \*1 Note : range depends on display mode : refer to the manual for details.

## (4) Bus Cycle Time / Instruction-Cycle Time

| Bus cycle time | Instruction cycle time | Clock divider | System clock oscillation                | Oscillation Frequency | Voltage      |
|----------------|------------------------|---------------|---|-----------------------|--------------|
| 0.424μs        | 0.848μs                | 1/2           | Internal VCO<br>(Ref : X'tal 32.768kHz) | 14.156MHz             | 4.5V to 5.5V |
| 7.5μs          | 15.0μs                 | 1/2           | Internal RC                             | 800kHz                | 4.5V to 5.5V |
| 91.55μs        | 183.1μs                | 1/1           | Crystal                                 | 32.768kHz             | 4.5V to 5.5V |
| 183.1μs        | 366.2μs                | 1/2           | Crystal                                 | 32.768kHz             | 4.5V to 5.5V |

## (5) Ports

- Input / Output Ports : 4 ports (24 terminals)
    - Data direction programmable in nibble units : 1 port (8 terminals)
- (If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)
- Data direction programmable for each bit individually : 3 ports (16 terminals)

- (6) AD converter
  - 4 channels × 6-bit AD converters
  
- (7) Serial interfaces
  - IIC-bus compliant serial interface (Multi-master type)  
Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.
  
- (8) PWM output
  - 3 channels × 7-bit PWM
  
- (9) Timer
  - Timer 0 : 16-bit timer/counter
    - With 2-bit prescaler + 8-bit programmable prescaler
    - Mode 0 : Two 8-bit timers with a programmable prescaler
    - Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
    - Mode 2 : 16-bit timer with a programmable prescaler
    - Mode 3 : 16-bit counter
    - The resolution of timer is 1 tCYC.
  - Timer 1 : 16-bit timer/PWM
    - Mode 0 : Two 8-bit timers
    - Mode 1 : 8-bit timer + 8-bit PWM
    - Mode 2 : 16-bit timer
    - Mode 3 : a variable-bit PWM (9 to 16 bits)
    - In mode 0/1, the resolution of timer/PWM is 1 tCYC
    - In mode 2/3, the resolution of timer/PWM is selectable by program; tCYC or 1/2 tCYC
  - Base timer
    - Generate every 500ms overflow for a clock application (using 32.768kHz crystal oscillation for the base timer clock)
    - Generate every 976μs, 3.9ms, 15.6ms, 62.5ms overflow (using 32.768kHz crystal oscillation for the base timer clock)
    - Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0
  
- (10) Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)
  - Noise rejection function
  - Polarity switching
  
- (11) Watchdog timer
  - External RC circuit is required
  - Interrupt or system reset is activated when the timer overflows
  
- (12) ROM correction function
  - Max 128 bytes / 2 addresses

## (13) Interrupts

- 12 sources 8 vectored interrupts
  1. External Interrupt INT0
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H, Timer T1L
  7. Vertical synchronous signal interrupt ( $\overline{VS}$ ), horizontal line ( $\overline{HS}$ )
  8. IIC

- Interrupt priority control

Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 8 listed above. For the external interrupt INT0 and INT1, low or highest priority can be set.

## (14) Sub-routine stack level

- A maximum of 128 levels (stack is built in the internal RAM)

## (15) Multiplication/division instruction

- 16 bits  $\times$  8 bits (7 instruction cycle times)
- 16 bits / 8 bits (7 instruction cycle times)

## (16) 3 oscillation circuits

- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

## (17) Standby function

- HALT mode

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request or the system reset.

- HOLD mode

The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.

- Pull the reset terminal ( $\overline{RES}$ ) to low level.
- Feed the selected level to either P70/INT0 or P71/INT1.

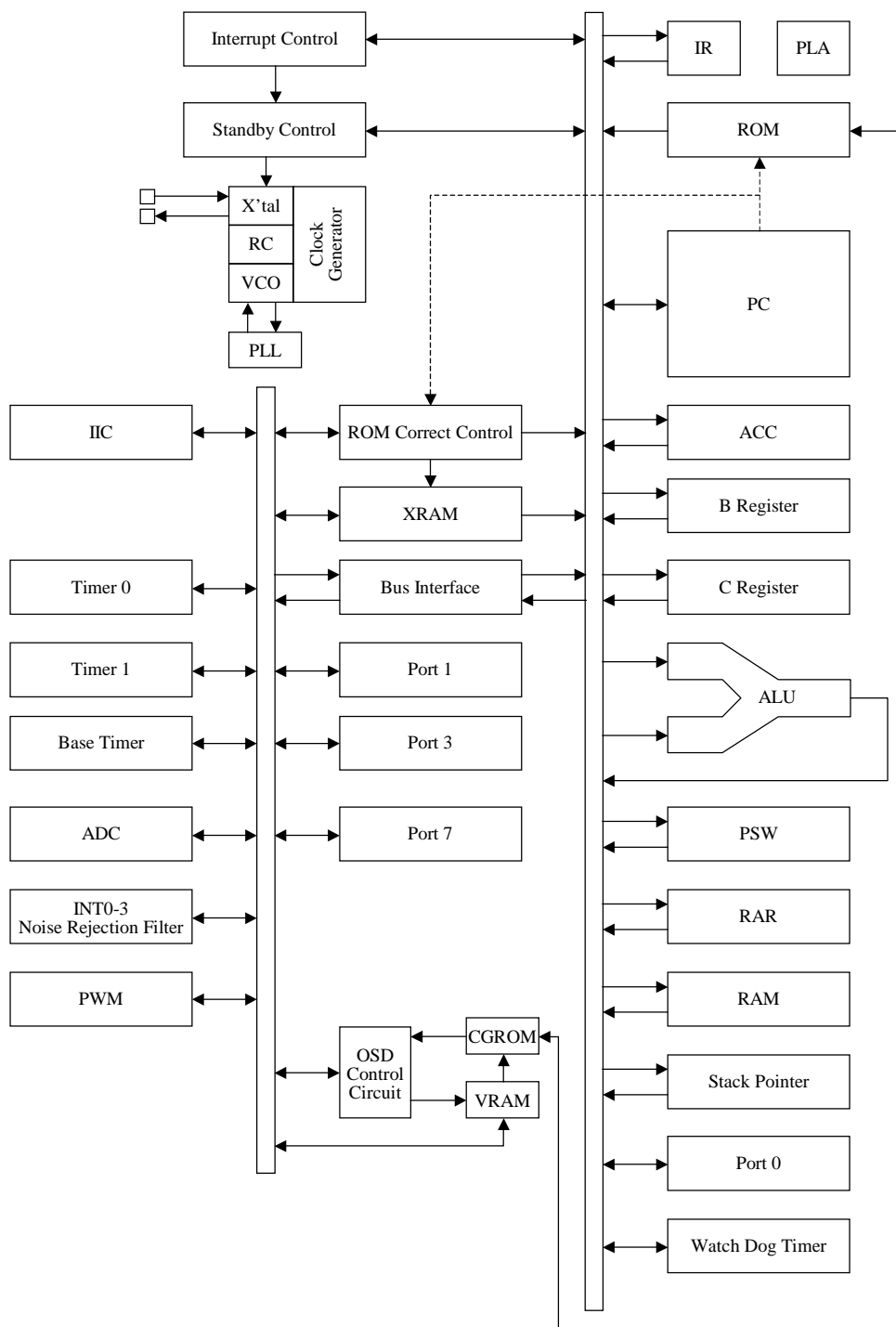
## (18) Package

- MFP36S
- DIP36S

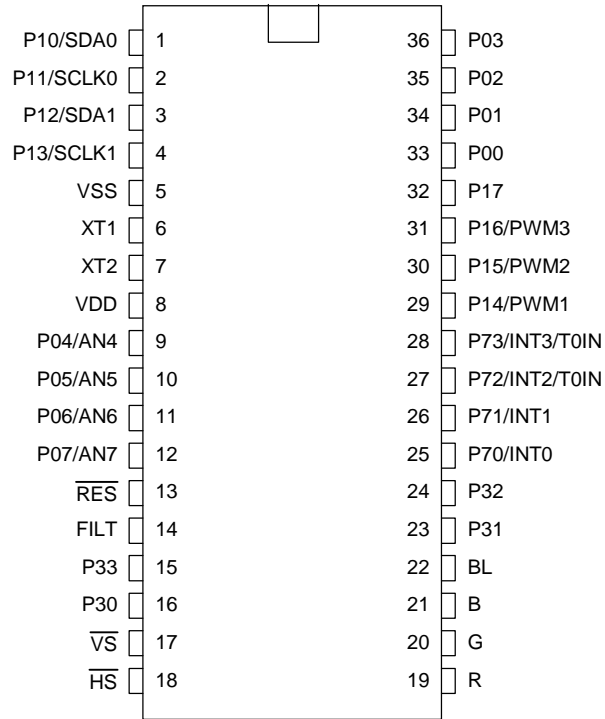
## (19) Development tools

- Flash EEPROM: LC86F3548A
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863400 (evaluation chip board)
  - + POD36-CABLE (cable)
  - + POD36-DIP (for DIP36S)
  - or POD36-MFP (for MFP36S)

System Block Diagram



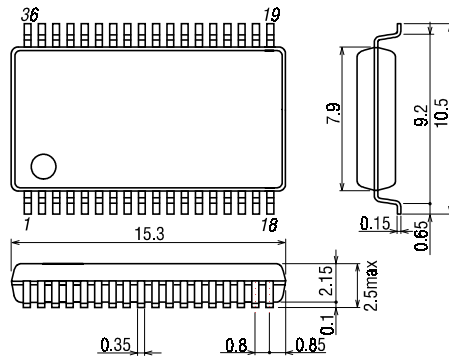
Pin Assignment



Package Dimension

(unit : mm)

3204

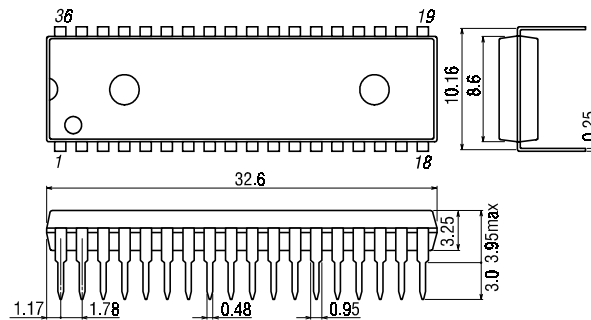


SANYO : MFP-36S

Package Dimension

(unit : mm)

3170



SANYO : DIP-36S

## Pin Description

Pin Description Table

| Terminal                | I/O                  | Function Description   | Option  |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
|-------------------------|----------------------|--|---|---------------|-----|-------------------|-----|---------------|-----|-------------------|-----|-------------|-----|-------------|-----|-------------|-----|----------------------|---------------------------|
| VSS                     | -                    | Negative power supply  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| XT1                     | I                    | Input terminal for crystal oscillator  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| XT2                     | O                    | Output terminal for crystal oscillator   |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| VDD                     | -                    | Positive power supply  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| $\overline{\text{RES}}$ | I                    | Reset terminal   |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| FILT                    | O                    | Filter terminal for PLL  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| $\overline{\text{VS}}$  | I                    | Vertical synchronization signal input terminal   |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| $\overline{\text{HS}}$  | I                    | Horizontal synchronization signal input terminal   |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| R                       | O                    | Red (R) output terminal of RGB image output  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| G                       | O                    | Green (G) output terminal of RGB image output  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| B                       | O                    | Blue (B) output terminal of RGB image output   |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| BL                      | O                    | Fast blanking control signal<br>Switch TV image signal and caption/OSD image signal  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| Port 0<br>P00 to P07    | I/O                  | <ul style="list-style-type: none"> <li>•8-bit input/output port,<br/>Input/output can be specified in nibble unit<br/>(If the N-ch open drain output is selected by option, the corresponding port data can be read in output mode.)</li> <li>•Other functions<br/>AD converter input port (P04 to P07: 4 channels)</li> </ul>   | Pull-up resistor provided/not provided<br>Output Format CMOS/Nch-OD |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| Port 1<br>P10 to P17    | I/O                  | <ul style="list-style-type: none"> <li>•8-bit input/output port<br/>Input/output can be specified for each bit (programmable pull-up resistor provided)</li> <li>•Other functions</li> </ul> <table border="1" style="margin-left: 20px;"> <tr><td>P10</td><td>IIC0 data I/O</td></tr> <tr><td>P11</td><td>IIC0 clock output</td></tr> <tr><td>P12</td><td>IIC1 data I/O</td></tr> <tr><td>P13</td><td>IIC1 clock output</td></tr> <tr><td>P14</td><td>PWM1 output</td></tr> <tr><td>P15</td><td>PWM2 output</td></tr> <tr><td>P16</td><td>PWM3 output</td></tr> <tr><td>P17</td><td>Timer 1 (PWM) output</td></tr> </table> | P10   | IIC0 data I/O | P11 | IIC0 clock output | P12 | IIC1 data I/O | P13 | IIC1 clock output | P14 | PWM1 output | P15 | PWM2 output | P16 | PWM3 output | P17 | Timer 1 (PWM) output | Output Format CMOS/Nch-OD |
| P10                     | IIC0 data I/O        |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P11                     | IIC0 clock output    |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P12                     | IIC1 data I/O        |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P13                     | IIC1 clock output    |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P14                     | PWM1 output          |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P15                     | PWM2 output          |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P16                     | PWM3 output          |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| P17                     | Timer 1 (PWM) output |  |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |
| Port 3<br>P30 to P33    | I/O                  | <ul style="list-style-type: none"> <li>•4-bit input/output port<br/>Input/output can be specified for each bit (CMOS output/input with programmable pull-up resistor)</li> </ul>   |   |               |     |                   |     |               |     |                   |     |             |     |             |     |             |     |                      |                           |

| Terminal                    | I/O   | Function Description  | Option             |   |         |                               |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
|-----------------------------|---|---|--------------------|---|---------|-------------------------------|-----|--------------------------------|-----|---|--|--------|---------|--------------------|---------|---------|--------|------|--------|--------|---------|--------|--------|-----|------|--------|--------|---------|--------|--------|-----|------|--------|--------|--------|---------|---------|-----|------|--------|--------|--------|---------|---------|-----|--|
| Port 7<br>P70<br>P71 to P73 | I/O   | <p>•4-bit input/output port<br/>Input or output can be specified for each bit</p> <p>( P70: I/O with programmable pull-up resistor<br/>P71 to P73: CMOS output/input with programmable pull-up resistor )</p> <p>•Other function</p> <table border="1" style="margin-left: 20px;"> <tr> <td>P70</td> <td>INT0 input/HOLD release input/<br/>Nch-Tr. output for watchdog timer</td> </tr> <tr> <td>P71</td> <td>INT1 input/HOLD release input</td> </tr> <tr> <td>P72</td> <td>INT2 input/Timer 0 event input</td> </tr> <tr> <td>P73</td> <td>INT3 input (noise rejection filter connected)/<br/>Timer 0 event input</td> </tr> </table> <p>Interrupt receiver format, vector addresses</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>rising</th> <th>falling</th> <th>rising/<br/>falling</th> <th>H level</th> <th>L level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table> | P70                | INT0 input/HOLD release input/<br>Nch-Tr. output for watchdog timer | P71     | INT1 input/HOLD release input | P72 | INT2 input/Timer 0 event input | P73 | INT3 input (noise rejection filter connected)/<br>Timer 0 event input |  | rising | falling | rising/<br>falling | H level | L level | vector | INT0 | enable | enable | disable | enable | enable | 03H | INT1 | enable | enable | disable | enable | enable | 0BH | INT2 | enable | enable | enable | disable | disable | 13H | INT3 | enable | enable | enable | disable | disable | 1BH |  |
| P70                         | INT0 input/HOLD release input/<br>Nch-Tr. output for watchdog timer   |   |                    |   |         |                               |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| P71                         | INT1 input/HOLD release input   |   |                    |   |         |                               |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| P72                         | INT2 input/Timer 0 event input  |   |                    |   |         |                               |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| P73                         | INT3 input (noise rejection filter connected)/<br>Timer 0 event input |   |                    |   |         |                               |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
|                             | rising  | falling   | rising/<br>falling | H level   | L level | vector                        |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| INT0                        | enable  | enable  | disable            | enable  | enable  | 03H                           |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| INT1                        | enable  | enable  | disable            | enable  | enable  | 0BH                           |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| INT2                        | enable  | enable  | enable             | disable   | disable | 13H                           |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |
| INT3                        | enable  | enable  | enable             | disable   | disable | 1BH                           |     |                                |     |   |  |        |         |                    |         |         |        |      |        |        |         |        |        |     |      |        |        |         |        |        |     |      |        |        |        |         |         |     |      |        |        |        |         |         |     |  |

Note: A capacitor of at least 10µF must be inserted between VDD and VSS when using this IC.

- Output form and existence of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.
- Port status in reset

| Terminal | I/O | Pull-up resistor status at selecting CMOS output option |
|----------|-----|---|
| Port 0   | I   | Pull-up resistor OFF, ON after reset release            |
| Port 1   | I   | Programmable pull-up resistor OFF                       |



1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

| Parameter                   | Symbol               | Pins                | Conditions        | Ratings                        |      |      | unit    |      |
|-----------------------------|----------------------|---------------------|-------------------|--------------------------------|------|------|---------|------|
|                             |                      |                     |                   | VDD[V]                         | min. | typ. |         | max. |
| Supply voltage              | VDDMAX               | VDD                 |                   |                                | -0.3 |      | +7.0    | V    |
| Input voltage               | VI(1)                | • RES, HS, VS, CVIN |                   |                                | -0.3 |      | VDD+0.3 |      |
| Output voltage              | VO(1)                | R, G, B, BL, FILT   |                   |                                | -0.3 |      | VDD+0.3 |      |
| Input/output voltage        | VIO                  | •Ports 0, 1, 3, 7   |                   |                                | -0.3 |      | VDD+0.3 |      |
| High level output current   | Peak output current  | IOPH(1)             | •Ports 0, 1, 3, 7 | •CMOS output<br>•For each pin. | -4   |      |         | mA   |
|                             |                      | IOPH(2)             | R, G, B, BL       | •CMOS output<br>•For each pin. | -5   |      |         |      |
|                             | Total output current | ΣIOAH(1)            | Ports 0, 1        | The total of all pins.         | -20  |      |         |      |
|                             |                      | ΣIOAH(2)            | Ports 3, 7        | The total of all pins.         | -10  |      |         |      |
|                             |                      | ΣIOAH(3)            | R, G, B, BL       | The total of all pins.         | -12  |      |         |      |
| Low level output current    | Peak output current  | IOPL(1)             | Ports 0, 1, 3     | For each pin.                  |      |      | 20      |      |
|                             |                      | IOPL(2)             | Port 7            | For each pin.                  |      |      | 15      |      |
|                             |                      | IOPL(3)             | R, G, B, BL       | For each pin.                  |      |      | 5       |      |
|                             | Total output current | ΣIOAL(1)            | Ports 0, 1        | The total of all pins.         |      |      | 40      |      |
|                             |                      | ΣIOAL(2)            | Ports 3, 7        | The total of all pins.         |      |      | 20      |      |
|                             |                      | ΣIOAL(3)            | R, G, B, BL       | The total of all pins.         |      |      | 12      |      |
| Maximum power dissipation   | Pdmax                | MFP36S              | Ta=-10 to +70°C   |                                |      |      | 340     | mW   |
|                             |                      | DIP36S              |                   |                                |      |      | 500     |      |
| Operating temperature range | Topg                 |                     |                   |                                | -10  |      | +70     | °C   |
| Storage temperature range   | Tstg                 |                     |                   |                                | -55  |      | +125    |      |

**LC863532A/28A/24A/20A/16A**

2. Recommended Operating Range at Ta=-10°C to +70°C, VSS=0V

| Parameter                      | Symbol  | Pins   | Conditions   | Ratings    |         |       | unit    |      |
|--------------------------------|---------|--|--|------------|---------|-------|---------|------|
|                                |         |  |  | VDD[V]     | min.    | typ.  |         | max. |
| Operating supply voltage range | VDD(1)  | VDD  | 0.844μs ≤ tCYC ≤ 0.852μs                           |            | 4.5     |       | 5.5     | V    |
|                                | VDD(2)  |  | 4μs ≤ tCYC ≤ 400μs                                 |            | 4.5     |       | 5.5     |      |
| Hold voltage                   | VHD     | VDD  | RAMs and the registers data are kept in HOLD mode. |            | 2.0     |       | 5.5     |      |
| High level input voltage       | VIH(1)  | Port 0   | Output disable                                     | 4.5 to 5.5 | 0.6VDD  |       | VDD     |      |
|                                | VIH(2)  | •Ports 1,3 (Schmitt)<br>•Port 7 (Schmitt) port input/interrupt<br>•HS, VS, RES (Schmitt) | Output disable                                     | 4.5 to 5.5 | 0.75VDD |       | VDD     |      |
|                                | VIH(3)  | Port 70 Watchdog timer input   | Output disable                                     | 4.5 to 5.5 | VDD-0.5 |       | VDD     |      |
| Low level input voltage        | VIL(1)  | Port 0   | Output disable                                     | 4.5 to 5.5 | VSS     |       | 0.2VDD  |      |
|                                | VIL(2)  | •Ports 1,3 (Schmitt)<br>•Port 7 (Schmitt) port input/interrupt<br>•HS, VS, RES (Schmitt) | Output disable                                     | 4.5 to 5.5 | VSS     |       | 0.25VDD |      |
|                                | VIL(3)  | Port 70 Watchdog timer input   | Output disable                                     | 4.5 to 5.5 | VSS     |       | 0.6VDD  |      |
| Operation cycle time           | tCYC(1) |  | •All functions operating                           | 4.5 to 5.5 | 0.844   | 0.848 | 0.852   | μs   |
|                                | tCYC(2) |  | •AD converter operating<br>•OSD is not operating   | 4.5 to 5.5 | 0.844   |       | 30      |      |
|                                | tCYC(3) |  | •OSD, AD converter is not operating                | 4.5 to 5.5 | 0.844   |       | 400     |      |
| Oscillation frequency range    | FmRC    |  | Internal RC oscillation                            | 4.5 to 5.5 | 0.4     | 0.8   | 3.0     | MHz  |

## 3. Electrical Characteristics at Ta=-10°C to +70°C, VSS=0V

| Parameter  | Symbol | Pins   | Conditions   | Ratings    |         |        | unit |      |
|--|--------|--|--|------------|---------|--------|------|------|
|  |        |  |  | VDD[V]     | min.    | typ.   |      | max. |
| High level input current                                     | IIH(1) | Ports 0, 1, 3, 7   | <ul style="list-style-type: none"> <li>•Output disable</li> <li>•Pull-up MOS Tr. OFF</li> <li>•VIN=VDD (including the off-leak current of the output Tr.)</li> </ul> | 4.5 to 5.5 |         |        | 1    | μA   |
|  | IIH(2) | <ul style="list-style-type: none"> <li>•<math>\overline{\text{RES}}</math></li> <li>•<math>\overline{\text{HS}}</math>, <math>\overline{\text{VS}}</math></li> </ul>                         | •VIN=VDD   | 4.5 to 5.5 |         |        | 1    |      |
| Low level input current                                      | IIL(1) | Ports 0, 1, 3, 7   | <ul style="list-style-type: none"> <li>•Output disable</li> <li>•Pull-up MOS Tr. OFF</li> <li>•VIN=VSS (including the off-leak current of the output Tr.)</li> </ul> | 4.5 to 5.5 | -1      |        |      |      |
|  | IIL(2) | <ul style="list-style-type: none"> <li>•<math>\overline{\text{RES}}</math></li> <li>•<math>\overline{\text{HS}}</math>, <math>\overline{\text{VS}}</math></li> </ul>                         | VIN=VSS  | 4.5 to 5.5 | -1      |        |      |      |
| High level output voltage                                    | VOH(1) | •CMOS output of ports 0,1,3,71-73  | IOH=-1.0mA   | 4.5 to 5.5 | VDD-1   |        |      | V    |
|  | VOH(2) | R, G, B, BL  | IOH=-0.1mA<br>R.G.B: digital mode  | 4.5 to 5.5 | VDD-0.5 |        |      |      |
| Low level output voltage                                     | VOL(1) | Ports 0,1,3,71-73  | IOL=10mA   | 4.5 to 5.5 |         |        | 1.5  |      |
|  | VOL(2) | Ports 0,3,71-73  | IOL=1.6mA  | 4.5 to 5.5 |         |        | 0.4  |      |
|  | VOL(3) | <ul style="list-style-type: none"> <li>•R, G, B, BL</li> <li>•Port 1</li> </ul>  | IOL=3.0mA<br>R.G.B: digital mode   | 4.5 to 5.5 |         |        | 0.4  |      |
|  | VOL(4) | Port 70  | IOL=1mA  | 4.5 to 5.5 |         |        | 0.4  |      |
| Pull-up MOS Tr. resistance                                   | Rpu    | •Ports 0, 1, 3, 7  | VOH=0.9VDD   | 4.5 to 5.5 | 13      | 38     | 80   | kΩ   |
| Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1) | RBS    | <ul style="list-style-type: none"> <li>•P10-P12</li> <li>•P11-P13</li> </ul>   |  | 4.5 to 5.5 |         |        | 130  | Ω    |
| Hysteresis voltage   | VHIS   | <ul style="list-style-type: none"> <li>•Ports 1, 3, 7</li> <li>•<math>\overline{\text{RES}}</math></li> <li>•<math>\overline{\text{HS}}</math>, <math>\overline{\text{VS}}</math></li> </ul> | Output disable   | 4.5 to 5.5 |         | 0.1VDD |      | V    |
| Pin capacitance  | CP     | All pins   | <ul style="list-style-type: none"> <li>•f=1MHz</li> <li>•Every other terminals are connected to VSS.</li> <li>•Ta=25°C</li> </ul>                                    | 4.5 to 5.5 |         | 10     |      | pF   |

4. IIC Input/Output Conditions at Ta=-10°C to +70°C, VSS=0V

| Parameter                             | Symbol  | Standard |      | High speed |      | unit |
|---------------------------------------|---------|----------|------|------------|------|------|
|                                       |         | min.     | max. | min.       | max. |      |
| SCL Frequency                         | fSCL    | 0        | 100  | 0          | 400  | kHz  |
| BUS free time between stop - start    | tBUF    | 4.7      | -    | 1.3        | -    | μs   |
| HOLD time of start, restart condition | tHD;STA | 4.0      | -    | 0.6        | -    | μs   |
| L time of SCL                         | tLOW    | 4.7      | -    | 1.3        | -    | μs   |
| H time of SCL                         | tHIGH   | 4.0      | -    | 0.6        | -    | μs   |
| Set-up time of restart condition      | tSU;STA | 4.7      | -    | 0.6        | -    | μs   |
| HOLD time of SDA                      | tHD;DAT | 0        | -    | 0          | 0.9  | μs   |
| Set-up time of SDA                    | tSU;DAT | 250      | -    | 100        | -    | ns   |
| Rising time of SDA, SCL               | tR      | -        | 1000 | 20+0.1Cb   | 300  | ns   |
| Falling time of SDA, SCL              | tF      | -        | 300  | 20+0.1Cb   | 300  | ns   |
| Set-up time of stop condition         | tSU;STO | 4.0      | -    | 0.6        | -    | μs   |

Refer to figure 7

(Note) Cb : Total capacitance of all BUS (unit : pF)

5. Pulse Input Conditions at Ta=-10°C to +70°C, VSS=0V

| Parameter                  | Symbol             | Pins  | Conditions   | Ratings    |      |      | unit |
|----------------------------|--------------------|---|--|------------|------|------|------|
|                            |                    |   |  | VDD[V]     | min. | typ. |      |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | •INT0, INT1<br>•INT2/T0IN                                     | •Interrupt acceptable<br>•Timer0-countable   | 4.5 to 5.5 | 1    |      | tCYC |
|                            | tPIH(2)<br>tPIL(2) | INT3/T0IN<br>(1 tCYC is selected for noise rejection clock.)  | •Interrupt acceptable<br>•Timer0-countable   | 4.5 to 5.5 | 2    |      |      |
|                            | tPIH(3)<br>tPIL(3) | INT3/T0IN<br>(16 tCYC is selected for noise rejection clock.) | •Interrupt acceptable<br>•Timer0-countable   | 4.5 to 5.5 | 32   |      |      |
|                            | tPIH(4)<br>tPIL(4) | INT3/T0IN<br>(64 tCYC is selected for noise rejection clock.) | •Interrupt acceptable<br>•Timer0-countable   | 4.5 to 5.5 | 128  |      |      |
|                            | tPIL(5)            | RES   | Reset acceptable   | 4.5 to 5.5 | 200  |      | μs   |
|                            | tPIH(6)<br>tPIL(6) | HS, VS  | •Display position controllable (Note)<br>•The active edge of HS and VS must be apart at least 1 tCYC.<br>•Refer to figure 6. | 4.5 to 5.5 | 8    |      |      |
| Rising/falling time        | tTHL<br>tTLH       | HS  | Refer to figure 6.   | 4.5 to 5.5 |      | 500  | ns   |

6. AD Converter Characteristics at Ta=-10°C to +70°C, VSS=0V

| Parameter                  | Symbol | Pins                                | Conditions                       | Ratings    |          |      | unit |      |     |
|----------------------------|--------|-------------------------------------|----------------------------------|------------|----------|------|------|------|-----|
|                            |        |                                     |                                  | VDD[V]     | min.     | typ. |      | max. |     |
| Resolution                 | N      |                                     |                                  | 4.5 to 5.5 |          | 6    |      | bit  |     |
| Absolute precision         | ET     |                                     | (Note)                           |            |          |      | ±1   |      | LSB |
| Conversion time            | tCAD   | Vref selection to conversion finish | 1 bit conversion time = 2 × Tcyc |            |          | 1.69 |      |      | µs  |
| Analog input voltage range | VAIN   | AN4 - AN7                           |                                  |            |          | VSS  |      | VDD  | V   |
| Analog port input current  | IAINH  |                                     |                                  |            | VAIN=VDD |      |      | 1    |     |
|                            | IAINL  |                                     |                                  | VAIN=VSS   |          | -1   |      |      |     |

(Note) Absolute precision does not include quantizing error (1/2LSB).

7. Analog Mode RGB Characteristics at Ta=-10°C to +70°C, VSS=0V

| Parameter             | Symbol | Pins                        | Conditions       | Ratings |      |      | unit |      |
|-----------------------|--------|-----------------------------|------------------|---------|------|------|------|------|
|                       |        |                             |                  | VDD[V]  | min. | typ. |      | max. |
| Analog output voltage |        | R.G.B<br>Analog output mode | Low level output | 5.0     | 0.45 | 0.5  | 0.55 | V    |
|                       |        |                             | Intensity output |         | 0.90 | 1.0  | 1.10 |      |
|                       |        |                             | Hi level output  |         | 1.35 | 1.5  | 1.65 |      |
| Time setting          |        | R.G.B                       | 70%<br>10pf load |         |      |      | 50   | ns   |

8. Sample Current Dissipation Characteristics at Ta=-10°C to +70°C, VSS=0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored.

| Parameter  | Symbol     | Pins | Conditions   | Ratings    |      |      | unit |      |
|--|------------|------|--|------------|------|------|------|------|
|  |            |      |  | VDD[V]     | min. | typ. |      | max. |
| Current dissipation during basic operation<br>(Note 3) | IDDOP(1)   | VDD  | <ul style="list-style-type: none"> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•System clock : VCO</li> <li>•VCO for OSD operating</li> <li>•OSD is Digital mode</li> <li>•Internal RC oscillation stops</li> </ul>          | 4.5 to 5.5 |      | 14   | 25   | mA   |
|  | IDDOP(2)   | VDD  | <ul style="list-style-type: none"> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•System clock : VCO</li> <li>•VCO for OSD operating</li> <li>•OSD is Analog mode</li> <li>•Internal RC oscillation stops</li> </ul>           | 4.5 to 5.5 |      | 23   | 37   |      |
|  | IDDOP(3)   | VDD  | <ul style="list-style-type: none"> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•System clock : X'tal</li> <li>•VCO for system VCO for OSD, internal RC oscillation stop</li> <li>•Data slicer, AD converters stop</li> </ul> | 4.5 to 5.5 |      | 100  | 300  | μA   |
| Current dissipation in HALT mode<br>(Note 3)           | IDDHALT(1) | VDD  | <ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•System clock : VCO</li> <li>•VCO for OSD stops</li> <li>•Internal RC oscillation stops</li> </ul>                        | 4.5 to 5.5 |      | 5    | 10   | mA   |
|  | IDDHALT(2) | VDD  | <ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•VCO for system stops</li> <li>•VCO for OSD stops</li> <li>•System clock : Internal RC</li> </ul>                         | 4.5 to 5.5 |      | 360  | 1000 |      |
|  | IDDHALT(3) | VDD  | <ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•VCO for system stops</li> <li>•VCO for OSD stops</li> <li>•System clock : X'tal</li> </ul>                               | 4.5 to 5.5 |      | 40   | 200  |      |
| Current dissipation in HOLD mode<br>(Note 3)           | IDDHOLD    | VDD  | <ul style="list-style-type: none"> <li>•HOLD mode</li> <li>•All oscillation stops.</li> </ul>  | 4.5 to 5.5 |      | 0.05 | 20   | μA   |

(Note 3) The currents through the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

| Frequency | Manufacturer | Oscillator | Recommended circuit parameters |      |      |       | Operating supply voltage range | Oscillation stabilizing time |       | Notes |
|-----------|--------------|------------|--------------------------------|------|------|-------|--------------------------------|------------------------------|-------|-------|
|           |              |            | C1                             | C2   | Rf   | Rd    |                                | typ.                         | max   |       |
| 32.768kHz | Seiko Epson  | C-002RX    | 18pF                           | 18pF | open | 390kΩ | 4.5 to 5.5V                    | 1.00S                        | 1.50S |       |

Notes The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

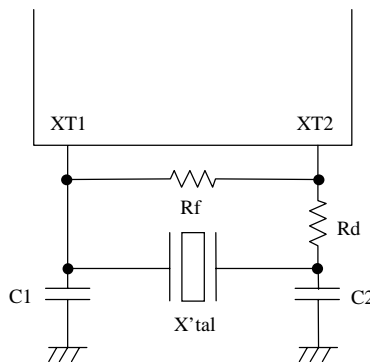


Figure 1 Recommended oscillation circuit.

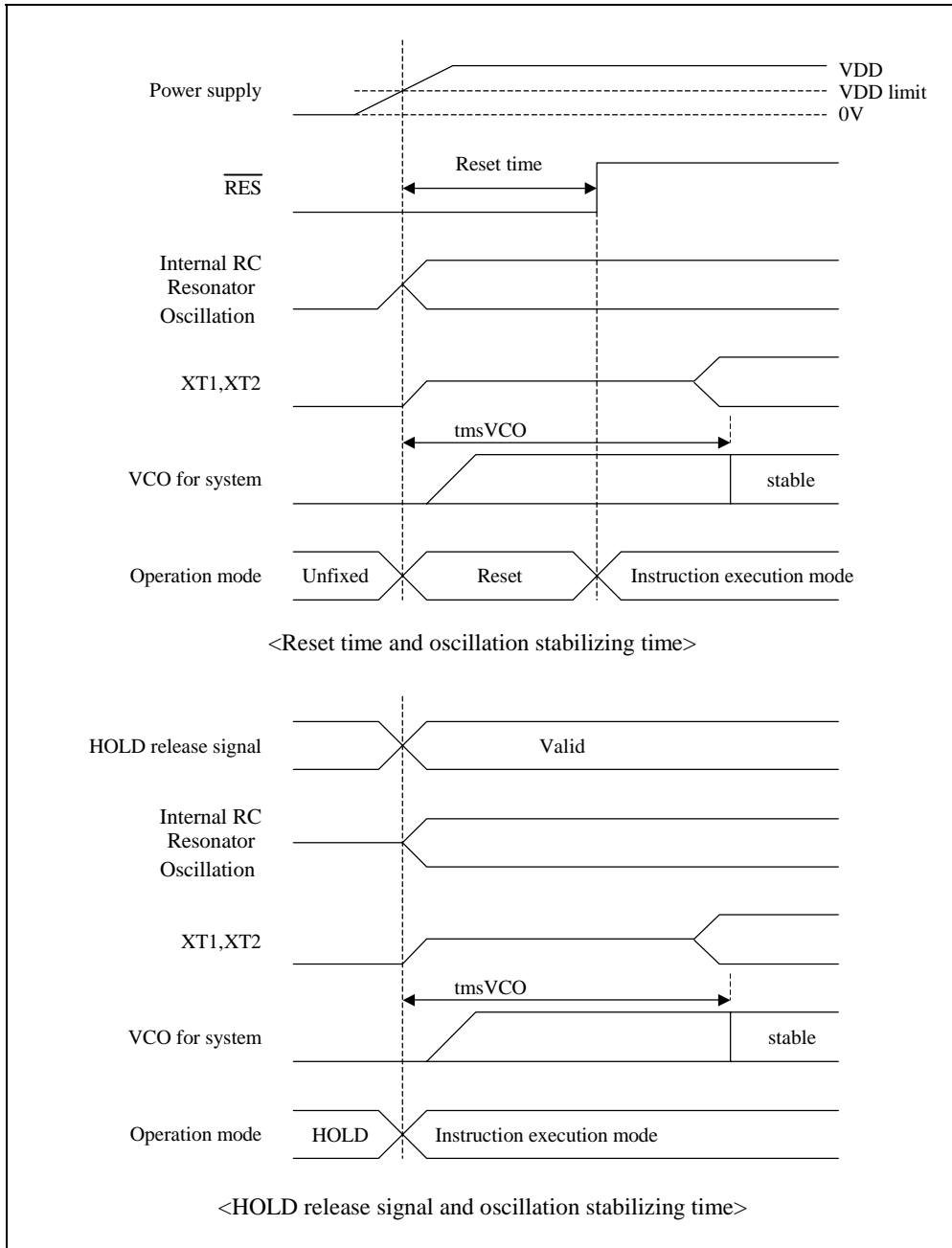


Figure 2 Oscillation stabilizing time



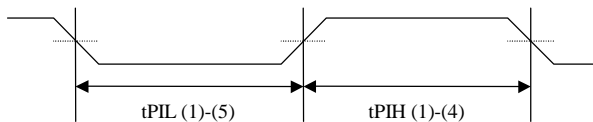


Figure 3 Pulse input timing condition - 1

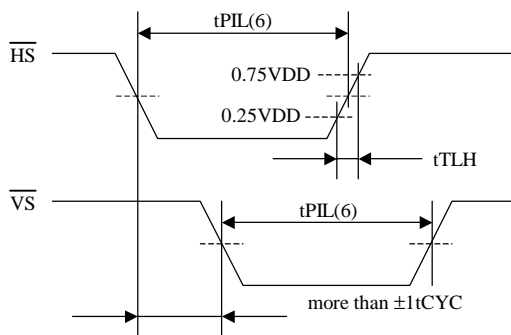


Figure 4 Pulse input timing condition - 2

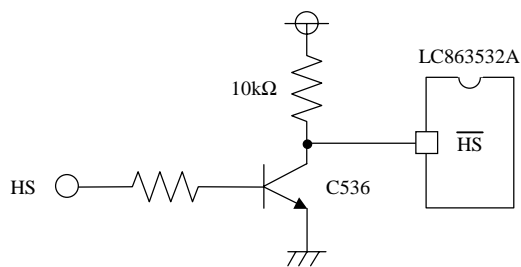


Figure 5 Recommended Interface circuit

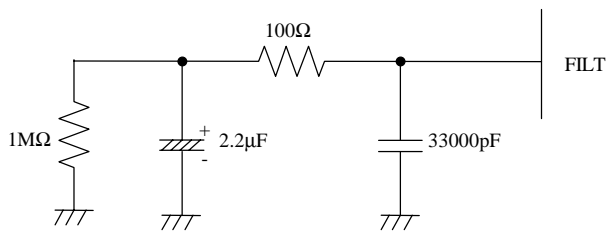
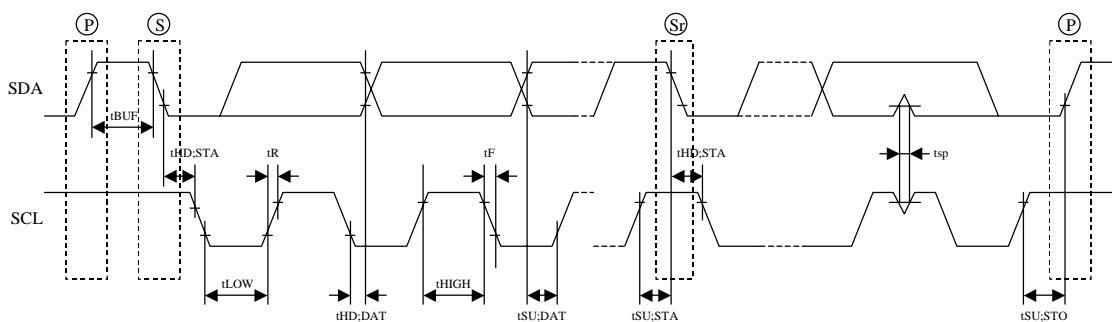


Figure 6 FILT recommended circuit

(Note) Place FILT parts on board as close to the microcontroller as possible.



S : start condition  
 P : stop condition  
 Sr : restart condition

tsp : Spike suppression

Standard mode : not exist  
 High speed mode : less than 50ns

Figure 7 IIC timing

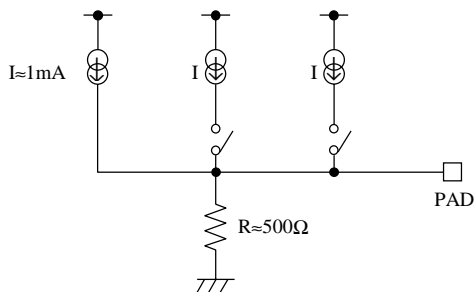


Figure 8 R.G.B. analog output equivalent circuit

memo :

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of December, 2000. Specifications and information herein are subject to change without notice.