Green-Mode PWM Controller with Frequency Swapping and Audio Noise Prevention

REV. 00

General Description

The LD5532 is built with several functions, audio noise prevention, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

It includes low startup current, green-mode power-saving operation, leading-edge blanking of the current sense and internal slope compensation. It also features protections of OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit from damage under abnormal conditions.

Furthermore, the Frequency Swapping function is also built-in to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

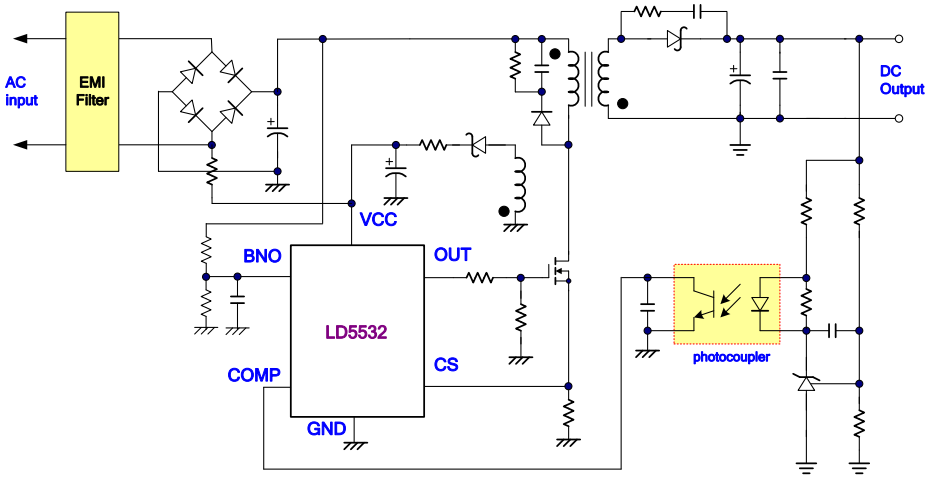
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<1.5μA)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- Brownout Protection
- OLP (Over Load Protection)
- 300mA/-500mA Driving Capability
- Grouping Frequency Limitation for Audio Noise

Applications

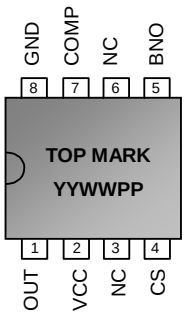
- LCD Monitor/TV Power
- Switching AC/DC Adaptor
- Open Frame Switching Power Supply

Typical Application

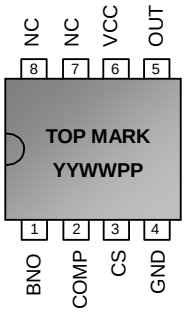


Pin Configuration

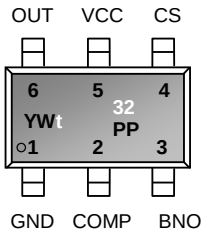
DIP-8 (TOP VIEW)



SOP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
t32 : LD5532

Ordering Information

Part number	Package	Top Mark	Shipping
LD5532 GL	SOT-26	YWt/32	3000 /tape & reel
LD5532 GS	SOP-8	LD5532 GS	2500 /tape & reel
LD5532 GN	DIP-8	LD5532 GN	3600 /tube /Carton

The LD5532 is ROHS compliant / Green Packaged

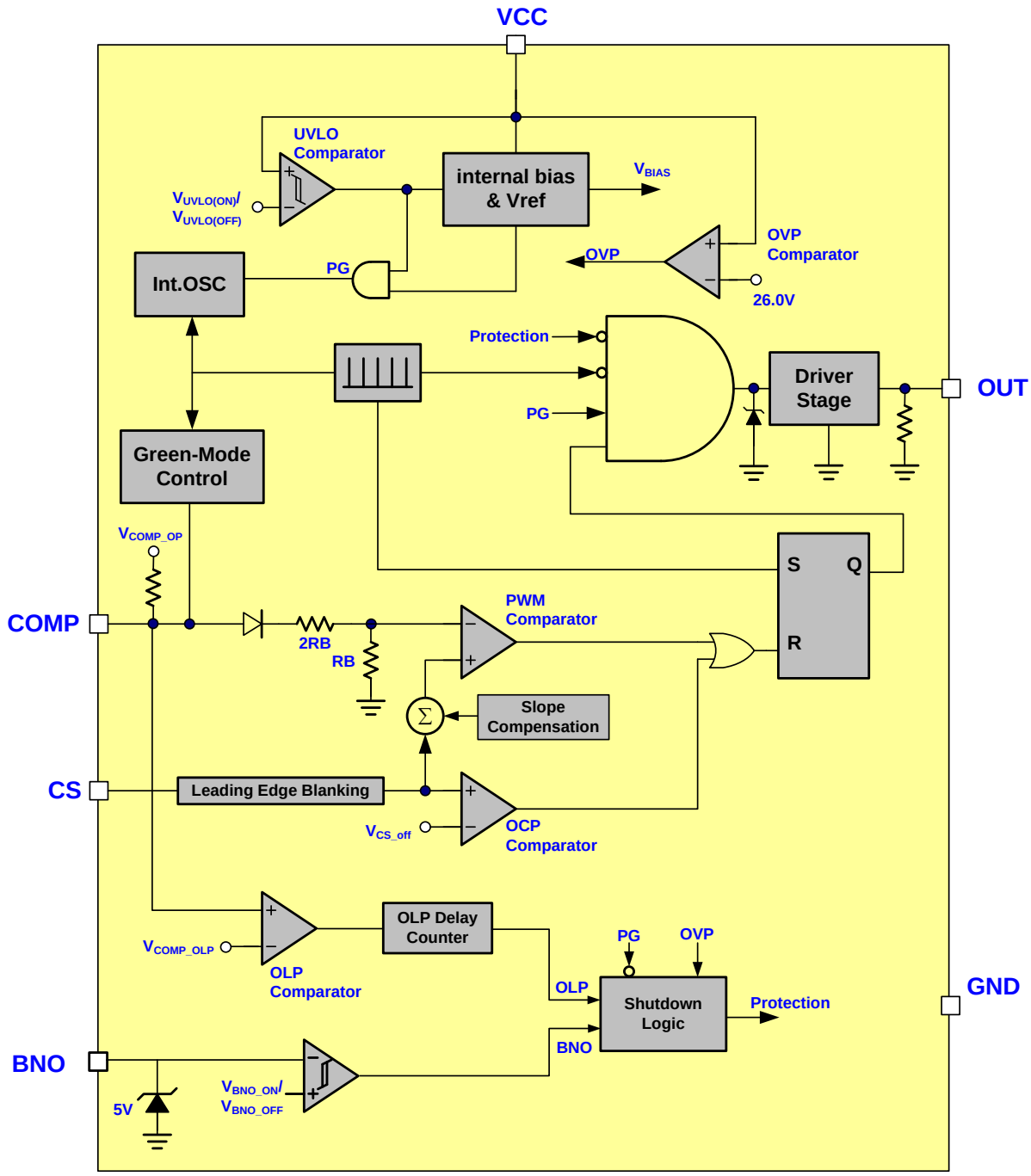
Protection Mode

Switching Freq.	VCC OVP	OLP	BNO Pin
65kHz	Auto recovery	Auto recovery/ 65ms	Auto recovery

Pin Descriptions

SOT-26	DIP-8	SOP-8	NAME	FUNCTION
1	8	4	GND	Ground
2	7	2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	5	1	BNO	Brownout Protection Pin. Connect a resistor divider between this pin and bulk capacitor voltage to set the brownout level. If the voltage below the threshold, the PWM output will be disabled.
4	4	3	CS	Current sense pin, connect it to sense the MOSFET current
5	2	6	VCC	Supply voltage pin
6	1	5	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3 ~29V
COMP, BNO, CS	-0.3 ~6V
OUT	-0.3 ~Vcc+0.3
Maximum Junction Temperature	150°C
Operating Junction Temperature	-40°C to 120°C
Operating Ambient Temperature	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	250°C/W
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation, PD@85°C (SOT-26)	160mW
Power Dissipation, PD@85°C (SOP-8)	250mW
Power Dissipation, PD@85°C (DIP-8)	650mW
Lead Temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	300mA/-500mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage Vcc	9.5V to 26V
Start-up Resistance	700K to 2.0MΩ
VCC Capacitor	10 to 47μF
COMP Capacitor Value	1~100nF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)						
Startup Current		I_{STUP}	0.1	0.4	1	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	I_{Vcc_0V}	0.55	0.625	0.675	mA
	V_{COMP}=3V	I_{Vcc_3V}	1.62	1.80	1.98	mA
	OLP Tripped	I_{OLP}		0.490		mA
	OVP Tripped	I_{OVP}		0.490		mA
UVLO (off)		$V_{UVLO(OFF)}$	7.5	8.5	9.5	V
UVLO (on)		$V_{UVLO(ON)}$	15	16	17	V
OVP Level		V_{OVP}	25	26	27	V
Voltage Feedback (Comp Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP_0V}	0.16	0.18	0.20	mA
Open Loop Voltage	COMP pin open	V_{COMP_OP}	5.00	5.20	5.40	V
Fixed Frequency Mode Threshold VCOMP(*)		V_{COMP_F}		2.20		V
Green Mode Threshold VCOMP(*)		V_{COMP_GN}		2.00		V
Burst Mode Threshold VCOMP		V_{BURST}		1.65		V
	Hysteresis	V_{BURST_H}		100		mV
Current Sensing (CS Pin)						
Maximum Input Voltage, V_{CS_Off}		V_{CS_OFF}	0.80	0.85	0.90	V
Minimum Input Voltage, V_{CS_min}		V_{CS_MIN}	0.6	0.65	0.7	V
Top Compensation Duty Ratio		D_{TOP}	49	51.6	54	%
Bottom Compensation Duty Ratio		D_{BOM}	17.7	18.6	19.5	%
Leading Edge Blanking Time		T_{LEB}		250		nS
Inter Slope Compensation	0% to D_{MAX}. (Linearly increase)	V_{SLOPE}	285	300	315	mV
Input impedance		Z_{IN}	1	--	10	MΩ
Delay to Output		T_D	50	100	150	nS

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Frequency, FREQ		F_{SW}	60	65	70	kHz
Green Mode Frequency, FREQG		F_{SW_GRN}	22	25	28	kHz
Trembling Frequency		F_{TRM}	3.0	4.0	5.0	kHz
Low Frequency period (FM)		F_L	200	220	240	Hz
Temp. Stability(*)		T_{STAB}	0	--	3	%
Voltage Stability(*)	(VCC=11V-25V)	V_{STAB}	0	--	1	%
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, Io=20mA	V_{O_L}	0	--	1	V
Output High Level	VCC=15V, Io=20mA	V_{O_H}	8	--	15	V
Rising Time(*)	Load Capacitance=1000pF	T_R	--	150	250	nS
Falling Time(*)	Load Capacitance=1000pF	T_F	--	50	100	nS
Max.Duty		D_{MAX}	70	75	80	%
OLP (Over Load Protection)						
OLP Trip Level		V_{COMP_OLP}	4.3	4.5	4.7	V
OLP Delay Time		T_{D_OLP}	58	65	72	mS
Brownout Protection (BNO Pin)						
Brownout turn-on Trip Level		V_{BNO_ON}	1.00	1.05	1.10	V
Brownout turn-off Trip Level		V_{BNO_OFF}	0.75	0.80	0.85	V
BNO Pin De-bounce Time		T_{D_BNO}	58	65	72	ms
On Chip OTP (Over Temperature) Auto-Recovery						
OTP Level(*)		T_{OTP}		145		°C
OTP Hysteresis(*)		T_{H_OTP}		20		°C
Soft-Start						
Soft-Start Duration	Enable	T_{SS}		6		ms

Notes:

*Guaranteed by design.

Typical Performance Characteristics

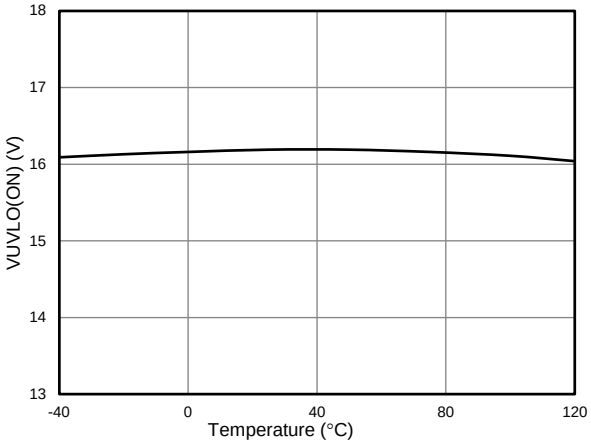


Fig. 1 UVLO(on) vs. Temperature

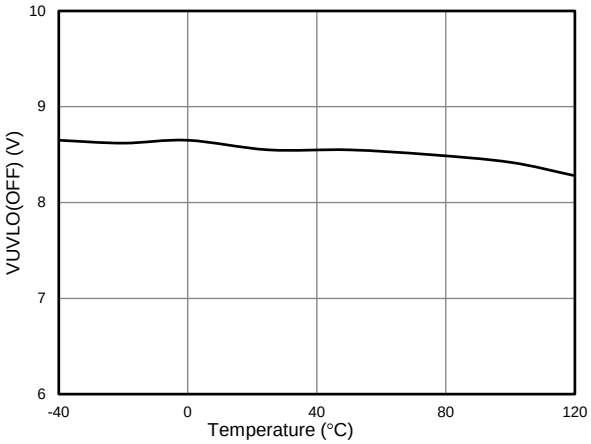


Fig. 2 UVLO(off) vs. Temperature

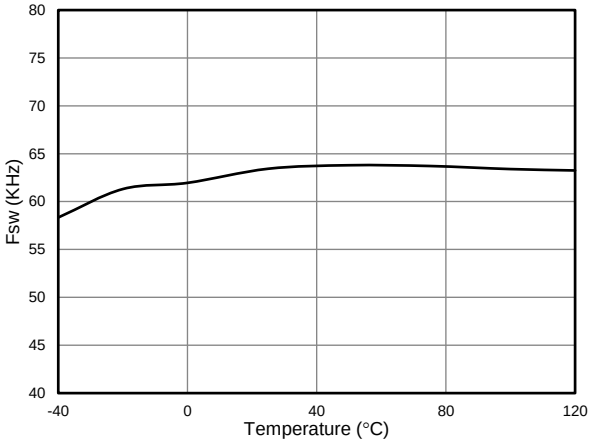


Fig. 3 Frequency vs.Temperature

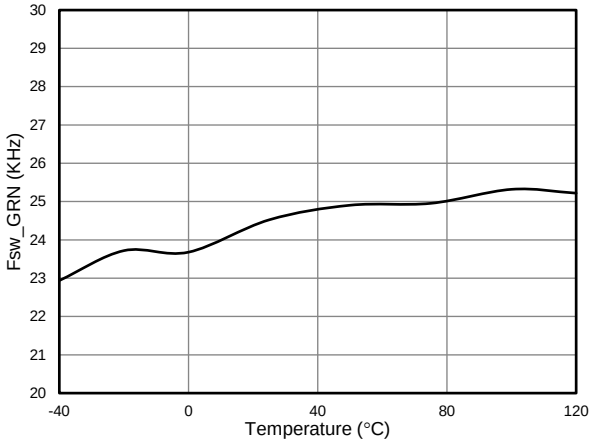


Fig. 4 Green Mode Frequency vs. Temperature

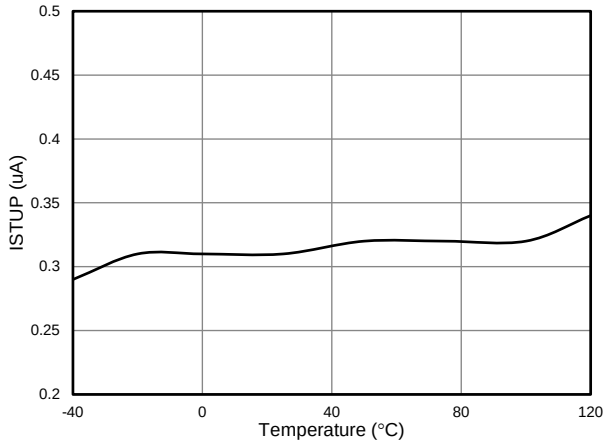


Fig. 5 VCC Startup Current vs. Temperature

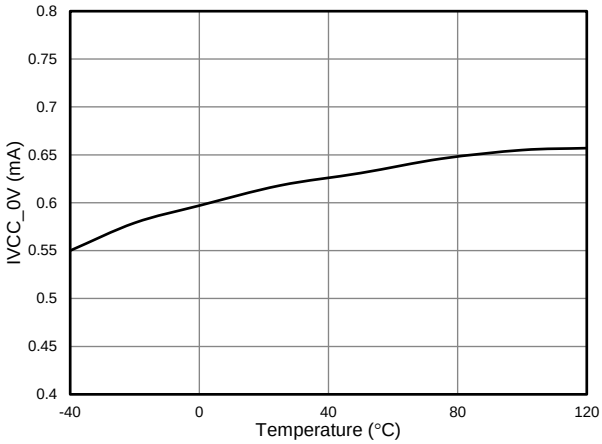


Fig. 6 Operating Current (VCOMP=0V) vs. Temperature

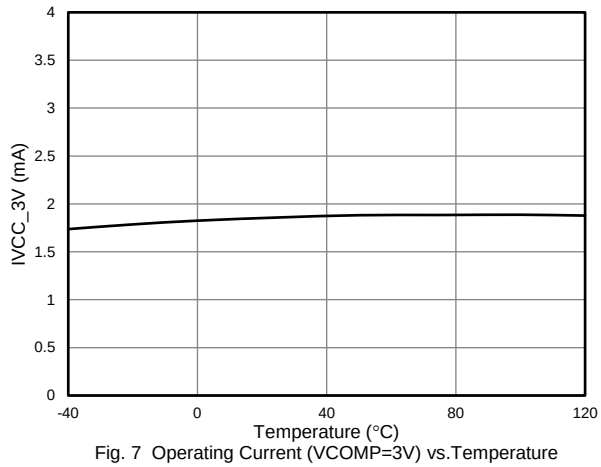


Fig. 7 Operating Current (VCOMP=3V) vs.Temperature

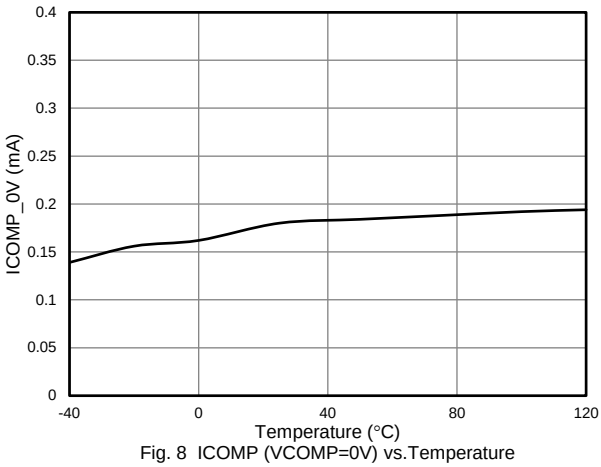


Fig. 8 ICOMP (VCOMP=0V) vs.Temperature

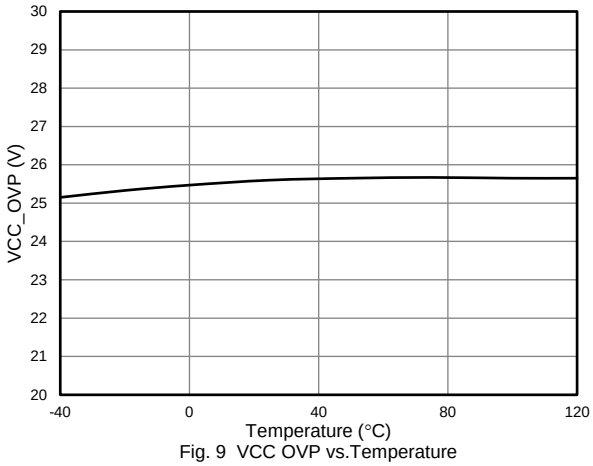


Fig. 9 VCC OVP vs.Temperature

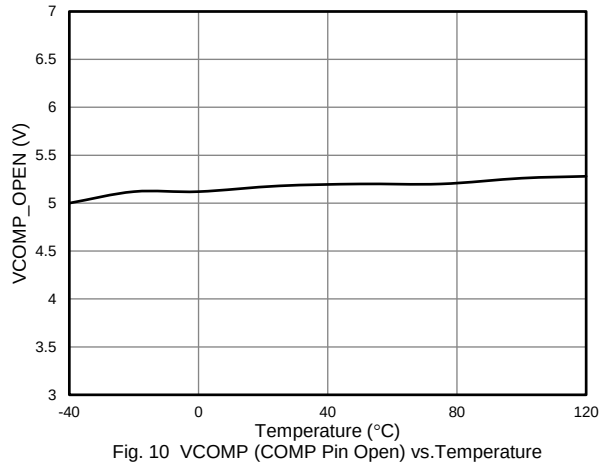


Fig. 10 VCOMP (COMP Pin Open) vs.Temperature

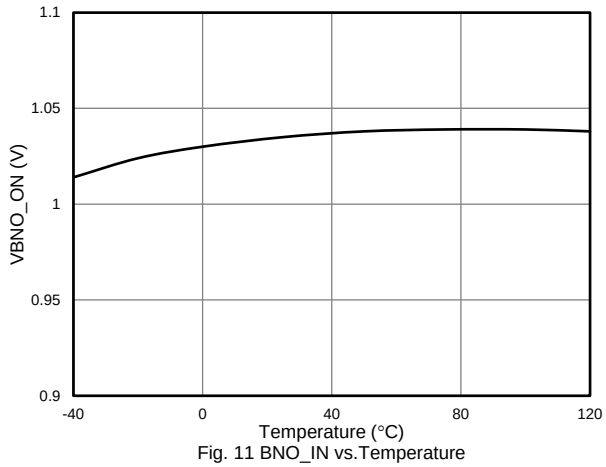


Fig. 11 BNO_IN vs.Temperature

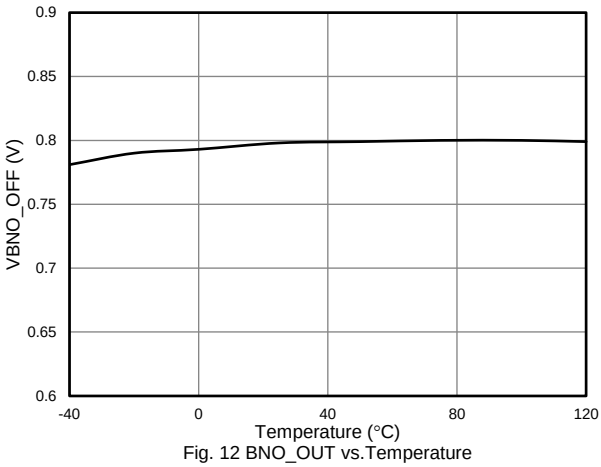


Fig. 12 BNO_OUT vs.Temperature

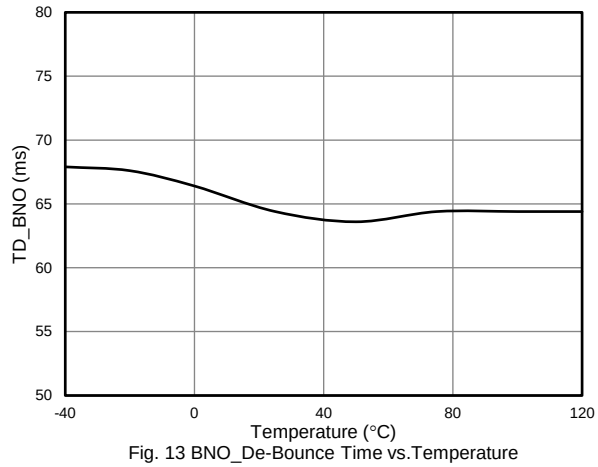


Fig. 13 BNO_De-Bounce Time vs.Temperature

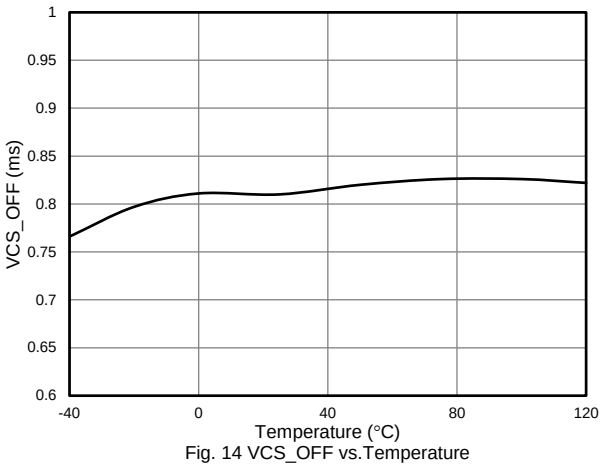


Fig. 14 VCS_OFF vs.Temperature

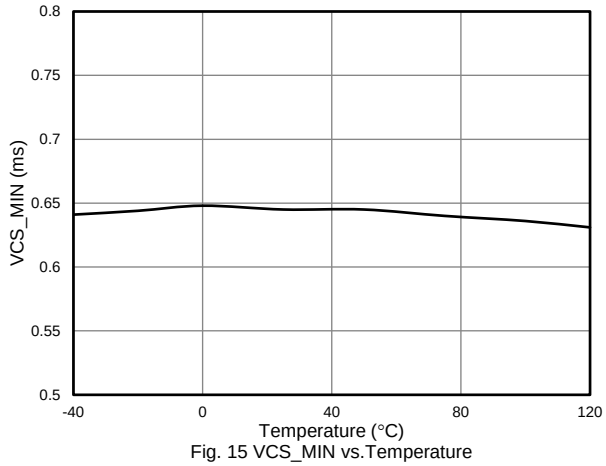


Fig. 15 VCS_MIN vs.Temperature

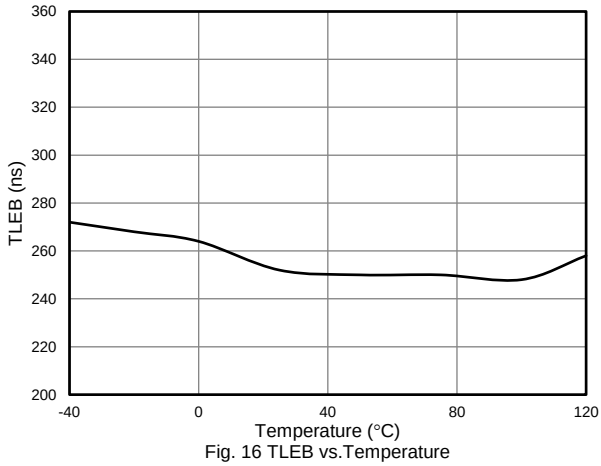


Fig. 16 TLEB vs.Temperature

Application Information

Operation Overview

The LD5532 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD5532 PWM controller and further to drive the power MOSFET. As shown in Fig. 17, a hysteresis is built in to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 8.0V, respectively.

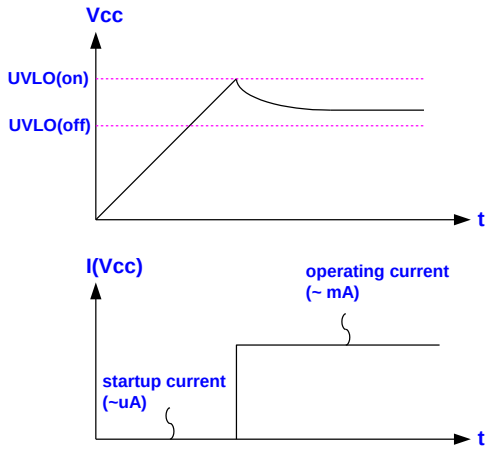


Fig. 17

Startup Current and Startup Circuit

The typical startup circuit to generate V_{CC} of the LD5532 is shown in Fig. 18. At the startup transient, the V_{CC} is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once V_{CC} obtains enough voltage to turn on the LD5532 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD5532 is only 0.6μA.

If a larger resistor of R1 is chosen, it will usually take more time to start up. A proper selection of R1 and C1 will optimize the power consumption and startup time.

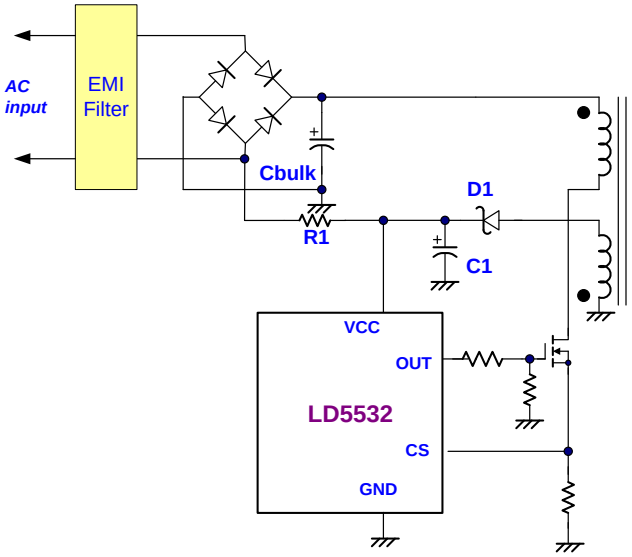


Fig. 18

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 19, the LD5532 detects the primary MOSFET current from the CS pin for the peak current mode control and also for the pulse-by-pulse current limit. The maximum voltage threshold of the current

sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

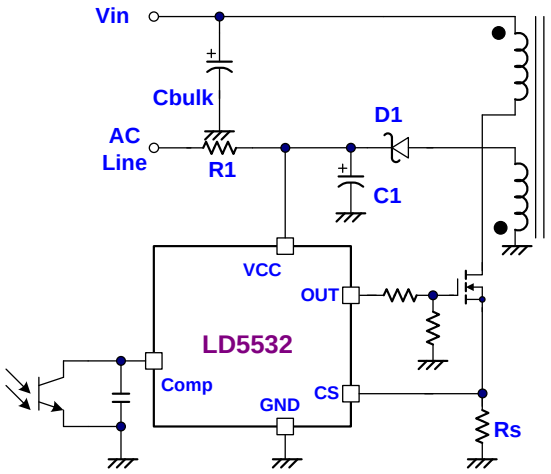


Fig. 19

A 250nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 250nS and the negative spike on the CS pin below -0.3V, the R-C filter is free to eliminate, as shown in Fig.20.

However, the total pulse width of the turn-on spike is determined according to output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 21) for larger power applications to avoid the CS pin being damaged by the negative turn-on spike.

Acoustic Noise Improvement Solution

The grouping frequency FG is set at 800Hz to prevent acoustic noise and also to limit the duty cycle in burst mode region.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5532 is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5532. Similar to UC3842, the LD5532 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of 2RB and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{2RB+RB} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

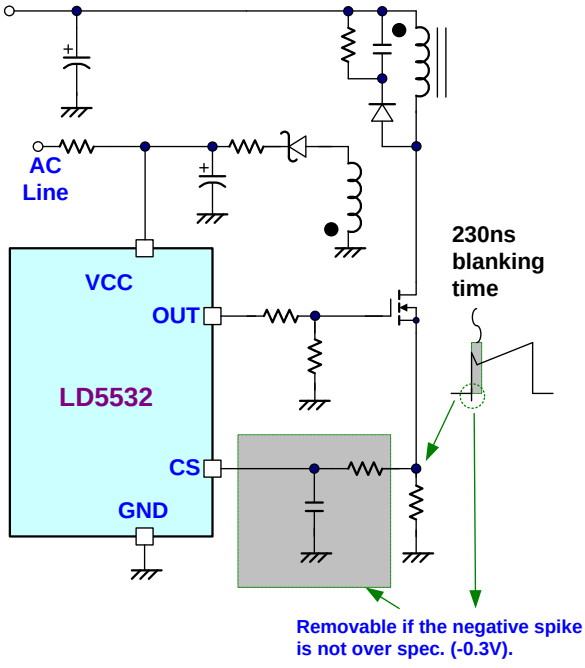


Fig. 20

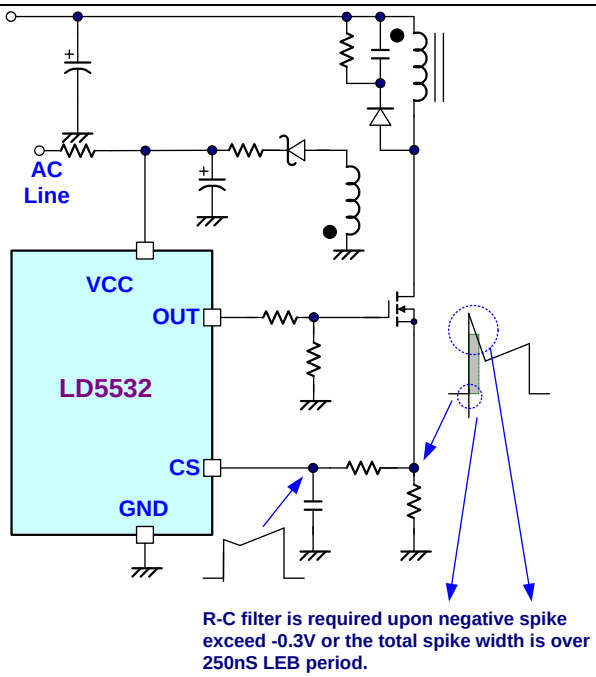


Fig. 21

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD5532 since it has integrated it already.

On/Off Control

The LD5532 can be turned off by pulling COMP pin below 1.5V. The gate output pin of the LD5532 will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to over-load condition, short or open-loop condition, the LD5532 is implemented with smart OLP function. It also features auto recovery function; see Fig. 22 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 4.5V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

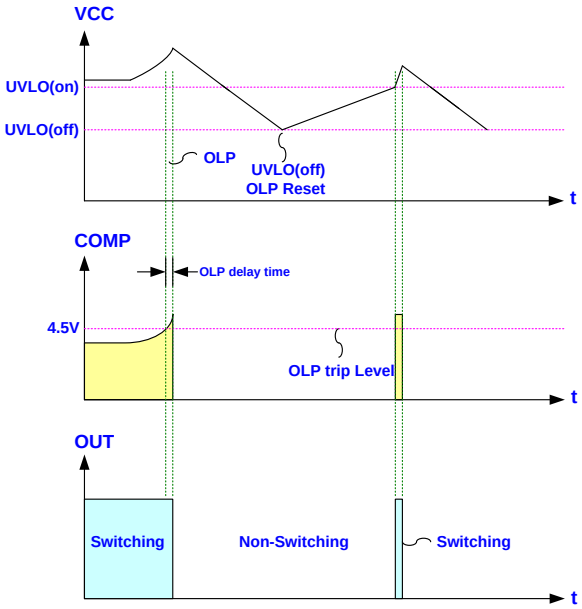


Fig. 22

OVP (Over Voltage Protection) on Vcc - Auto Recovery

The maximum VGS ratings of the power MOSFETs are mostly for 30V. To prevent the VGS from fault condition, LD5532 is implemented with OVP function on Vcc. If Vcc voltage is higher than the OVP threshold, the output gate drive circuit will be shut off simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

The Vcc OVP functions of LD5532 are auto-recoverable. Open-loop of feedback will usually activate the OVP. Before

it's released, the VCC will trip the OVP level again and re-shutdown the output in hiccup mode. Fig. 23 shows the operation.

Otherwise, when the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

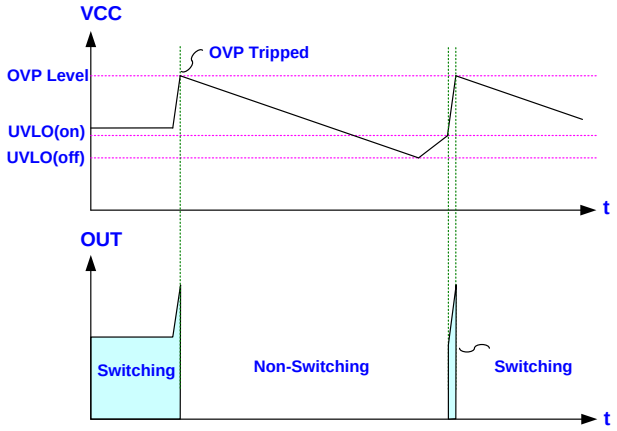


Fig. 23

Brownout Protection

The LD5532 is programmable for the brownout protection point though BNO pin. The voltage across the BNO pin is proportional to the bulk capacitor voltage, referred as the line voltage. A brownout comparator is implemented to detect the abnormal line condition. As soon as the condition is detected, it will shut down the controller to prevent the damage. Fig. 24 shows the operation. When VBNO falls below 0.80V, the gate output will remain off even as Vcc achieved UVLO(ON). It therefore makes Vcc hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage is large enough to pull VBNO over 1.05V, the gate output will not start switching even when the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false trigger during turn-on and turn-off.

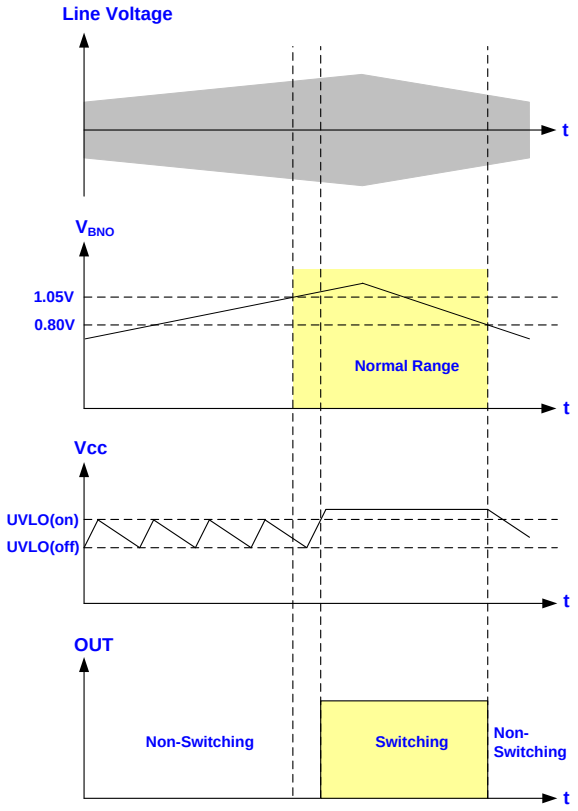


Fig. 24

Oscillator and Switching Frequency

The LD5532 is implemented with Frequency Swapping function which helps the power supply designers to optimize EMI performance in lower system cost. The switching frequency substantially centers at 65KHz, and swaps in the range of ±4KHz.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

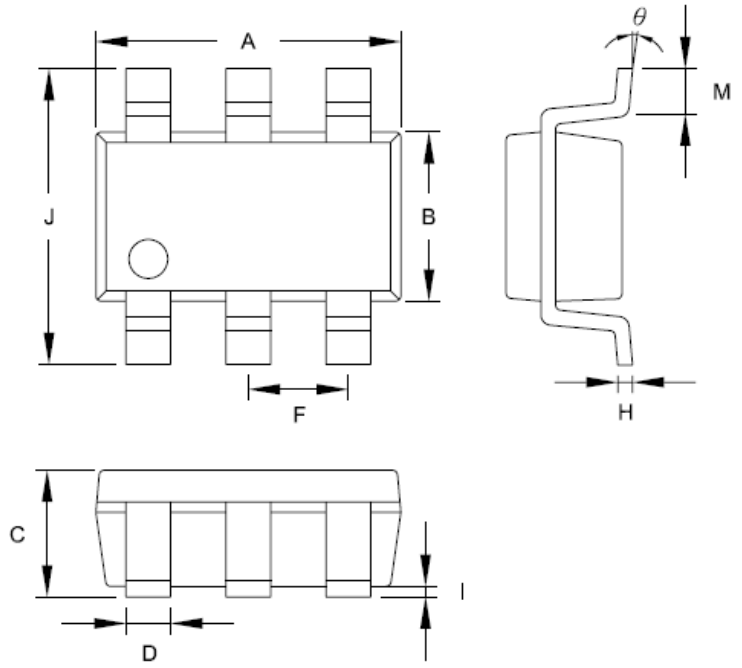
There are several critical protections integrated in the LD5532 to prevent from damage to the power supply. Those damages usually come from open or short conditions on of LD5532.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

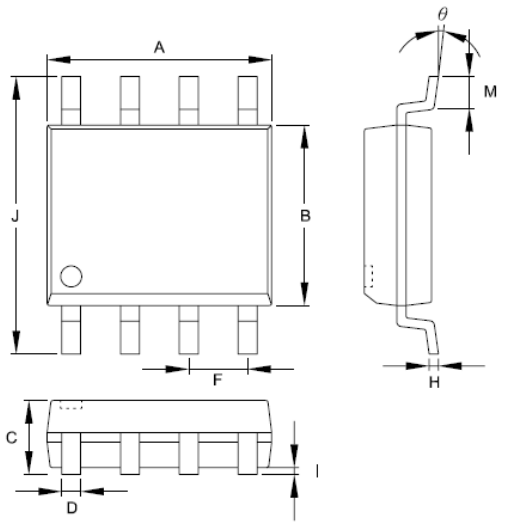
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

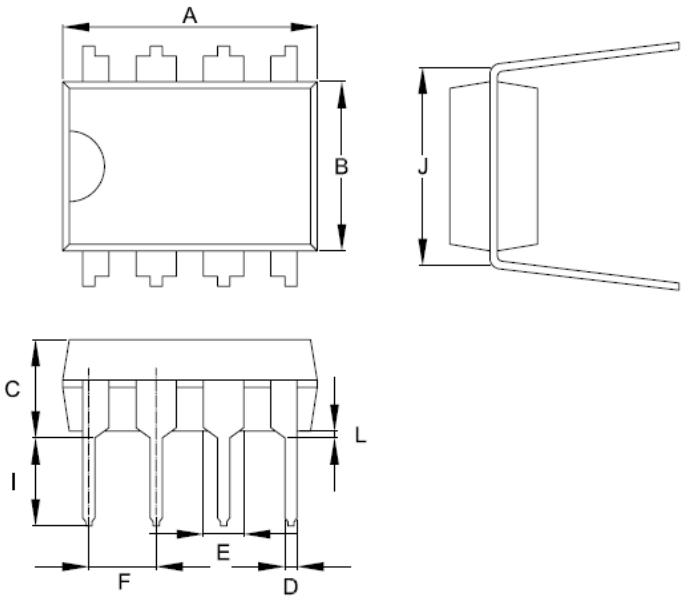
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	07/08/2014	Original Specification